INSTRUMENTATION AMPLIFIER APPLICATION GUIDE

2ND Edition

by

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and
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SECTION I—BASIC IN-AMP THEORY

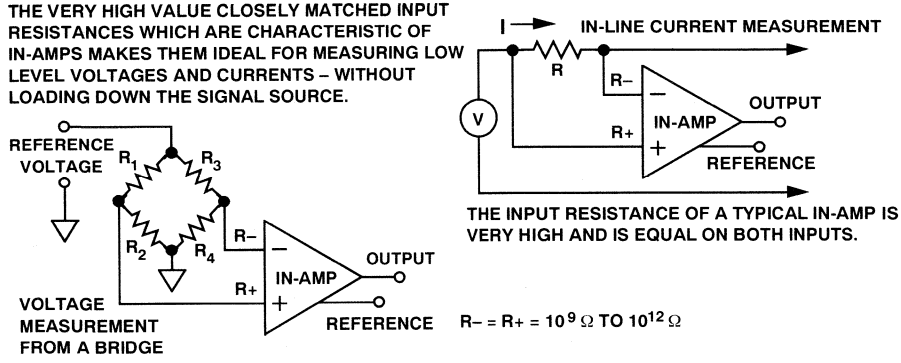
Introduction

The fact that some op-amps are dubbed instrumentation amplifiers (or in-amps) by their suppliers does not make them an in-amp, even though they may be used in instrumentation. Likewise, an isolation amplifier is also not an instrumentation amplifier. This application note will explain what an in-amp actually is, how it operates, and how and where to use it.

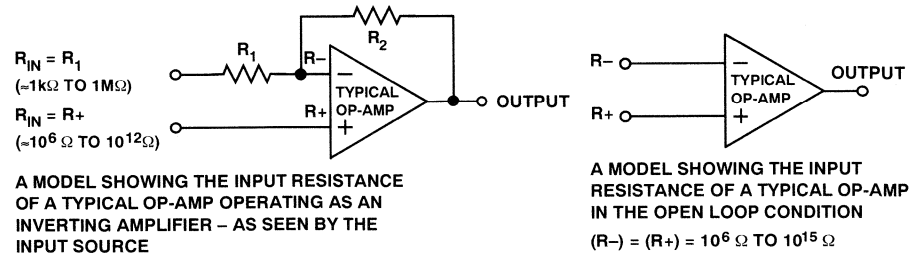
What Is an Instrumentation Amplifier?

An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is single-ended with respect to a reference terminal. Most commonly, the impedances of the two input terminals are balanced and have high values, typically $10^9\ \Omega$ or greater. As with op-amps, output impedance is very low, nominally only a few milliohms. Unlike an op-amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Figure 1 contrasts the differences between op-amp and in-amp input characteristics.

Common-mode rejection, the property of cancelling out any signals which are common (the same potential on both inputs) while amplifying any signals which are differential (a potential difference between the inputs), is the most important function an instrumentation amplifier provides. Common-mode gain (A_{CM}) is the ratio of change in output voltage to a change in common-mode input voltage. This is the net gain (or attenuation) from input to output for voltages common to both inputs. For example, an in-amp with a common-mode gain of 1/1,000 and a 10 volt common-mode voltage at its inputs will exhibit a 10 mV output change. The differential or "normal mode" gain (A_D) is the gain between input and output for voltages applied differentially (or across) the two inputs. The common-mode rejection ratio (CMRR) is simply the ratio of



IN-AMP INPUT CHARACTERISTICS



OP-AMP INPUT CHARACTERISTICS

Figure 1. Op-Amp vs. In-Amp Input Characteristics

the differential gain, A_D, to the common-mode gain (A_{CM}).

Common-mode rejection is usually specified for a full-range common-mode voltage (CMV) change at a given frequency, and a specified imbalance of source impedance (e.g., 1 kΩ source unbalance, at 60 Hz). The term CMR is a logarithmic expression of the common-mode rejection ratio (CMRR).

That is: CMR = 20 Log_{10} CMRR.

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals while simultaneously rejecting volts of common-mode at its inputs.

This requires that instrumentation amplifiers have very high common-mode rejection—typical values of CMR are 70 dB to over 100 dB, with CMR usually improving at higher gains. While it is true that operational amplifiers, connected as subtractors, also provide common-mode rejection, the user must provide closely matched external resistors. On the other hand, monolithic in-amps with their pretrimmed resistor networks, are far easier to apply.

What Other Properties Define a High Quality In-Amp?

Besides possessing a high common-mode rejection ratio, an instrumentation amplifier needs the following properties:

A. **A Matched, High Input Impedance.** The impedances of the inverting and noninverting input terminals of an in-amp must be high and closely matched to one another. Values of 10^9 Ω to 10^{12} Ω are typical.

B. **Low Noise.** Because it must be able to handle very low level input voltages, an in-amp must not add its own noise to that of the signal. An input noise level of 10 nV/$\sqrt{\text{Hz}}$ @ 1 kHz referred to input (RTI) or lower is desirable.

C. **Low Nonlinearity.** Input offset and scale factor errors can be corrected by external trimming; but, nonlinearity is an inherent performance limitation of the device which cannot be removed by external adjustment. Low nonlinearity must be designed-in by the in-amp manufacturer. Nonlinearity is normally specified in percent of full scale where the manufacturer measures the in-amp's error at the plus and minus full-scale voltage and at zero. A nonlinearity error of 0.01% is typical for a high quality in-amp; some even have levels as low as 0.0001%.

D. **Adequate Bandwidth.** An instrumentation amplifier must provide sufficient bandwidth needed for the particular application. Since typical unity gain small-signal bandwidths fall between 500 kHz and 4 MHz, performance at low gains is easily achieved, but at higher gains, bandwidth becomes much more of an issue.

F. **Simple Gain Selection.** Gain selection should be quick and easy to apply. Gain selection via a single external resistor is one common method. Many in-amps provide a choice of internally preset gains (often pin selectable) which are stable over temperature.

G. **Low Offset Voltage and Offset Voltage Drift.** As with an operational amplifier, an in-amp must have a low offset voltage. Since an instrumentation amplifier consists of two independent sections: an input stage and an output amplifier, total output offset will equal the sum of the gains, times the input offset, plus the output offset. Although the initial offset voltage may usually be nulled with external trimming, offset voltage drift cannot be adjusted out. As with initial offset, offset drift has two components, with both the input and output section of the in-amp each contributing its portion of error to the total. As gain is increased, the offset drift of the input stage becomes the dominant source of offset error. Values of 100 μV and 2 mV are typical values for input and output offset, respectively.

H. **Low Input Bias and Offset Current Errors.** Again, as with an op-amp, an instrumentation amplifier has *bias* currents which flow into, or out of, its input terminals: bipolar in-amps with their base currents and FET amplifiers with gate leakage currents. This *bias current* flowing through an imbalance in the signal source resistance will create an offset error. Note that if the input source resistance becomes very large—as with ac input coupling without a resistive return to power supply ground—the input common-mode voltage will climb until the amplifier saturates. A high value resistor, connected between each input and ground, is normally used to prevent this problem. Input *offset current* errors are defined as the mismatch between the bias currents flowing in the two

inputs. Typical values of input bias current for a bipolar in-amp range from 1 nA to 0.5 μA; for a FET input device, values of 50 pA are typical at room temperature.

Where Is an Instrumentation Amplifier Used?

Data Acquisition. In-amps find their primary use amplifying signals from low output level transducers in noisy environments. The amplification of pressure or temperature transducer signals is a common in-amp application. Common bridge applications include strain and weight measurement using "load cells" and temperature measurement using resistive temperature detectors or "RTD's."

Medical Instrumentation. In-amps are also widely used in medical equipment such as ECG & EEG monitors and blood pressure monitors.

Audio Applications. Again, because of their high common-mode rejection, instrumentation amplifiers are sometimes used for audio (as microphone preamps, etc.) to extract a weak signal from a noisy environment and to minimize offsets and noise due to ground loops.

High Speed Signal Conditioning. As the speed and accuracy of modern video data acquisition systems have increased, there has developed a growing need for high bandwidth instrumentation amplifiers—particularly in the field of CCD imaging equipment where offset correction and input buffering are required. Here double-correlated sampling techniques are often used for offset correction of the CCD image. Two sample-and-hold amplifiers monitor the pixel and reference levels, and a dc corrected output is provided by feeding their signals into an instrumentation amplifier.

In-Amps: an External View

Figure 2, shows a functional block diagram of an instrumentation amplifier.

Since an ideal instrumentation amplifier detects only the difference in voltage between its inputs, any common-mode signals (potentials which are equal on both inputs), such as noise or voltage drops in ground lines, are rejected at the input stage without being amplified.

Normally, either a single resistor or resistor pair is used to program the in-amp for the desired gain. The manufacturer will then provide a transfer function or gain equation that allows the user to calculate the required values of resistance for a given gain.

The output of an instrumentation amplifier has its own reference terminal which allows it to drive ground referenced loads, such as those usually found in instruments. Figure 2 shows the input and output commons being returned to the same point where they are connected to power supply "ground." This "star" ground connection is a very effective means for minimizing ground loops in the circuit; however some residual "common-mode"

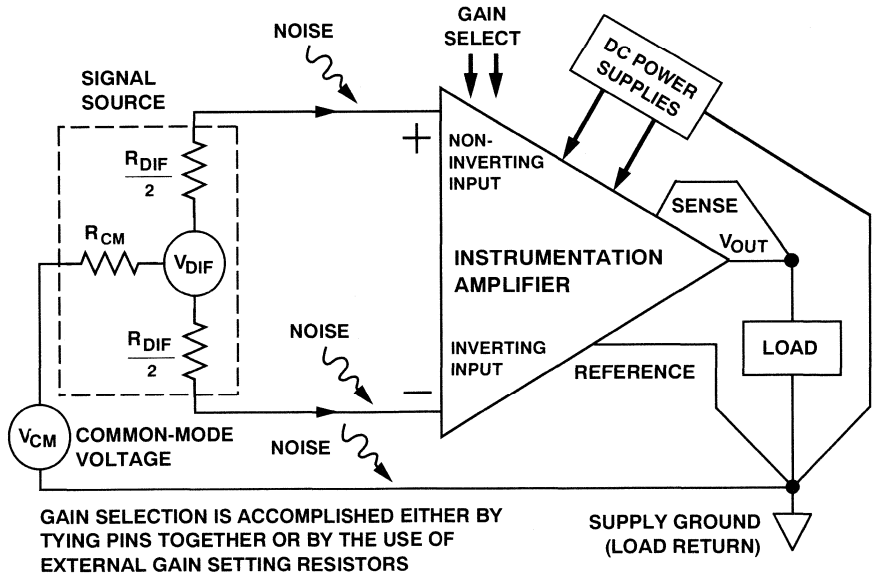


Figure 2. Basic Instrumentation Amplifier

ground currents will still remain. These currents flowing through R_{CM} will develop a common-mode voltage error, V_{CM}. The in-amp, by virtue of its high common-mode rejection, will amplify the differential signal while rejecting V_{CM} and any common-mode noise.

Of course, power must be supplied to the IA—as with op-amps, this is normally a dual supply voltage which will operate the in-amp over a specified range. Alternatively, only a single ground referenced supply may be required, for some in-amps.

An instrumentation amplifier may be assembled using one or more operational amplifiers or it may be of monolithic design. Both approaches have their virtues and limitations. In general, op-amp in-amps offer wide flexibility at low cost and sometimes can provide performance unattainable from monolithic designs, such as in very high bandwidth applications. In contrast, monolithic designs provide the complete in-amp function, fully specified and, in many cases, factory trimmed to high accuracy. Op-amp designs will be discussed first.

Inside an Instrumentation Amplifier

A Simple Op-Amp Subtractor Provides an In-Amp Function. The most simple (and very useful) method of implementing a differential gain block is shown in Figure 3.

If $R_1 = R_3$ and $R_2 = R_4$, then:

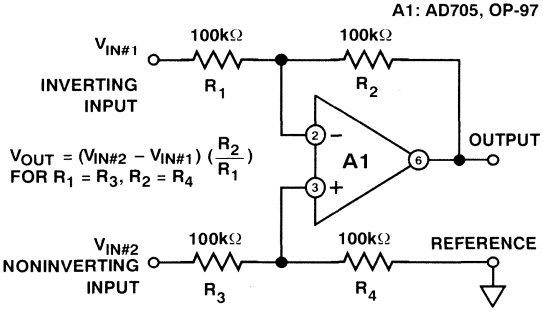


Figure 3. A One Op-Amp IA Circuit Functional Diagram

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1}) \left(\frac{R_2}{R_1}\right)$$

Although this circuit does provide an in-amp function—amplifying differential signals while rejecting those which are common-mode—it also has some serious limitations. To start with, the impedances of the inverting and noninverting inputs are relatively low and unequal. In this example, the input impedance to $V_{IN\#1}$ equals 100 kΩ, while the impedance of $V_{IN\#2}$ is twice that, equaling 200 kΩ. Therefore, when you apply a voltage to one input, while grounding the other, you will have different currents flowing depending on which input receives the applied voltage.

Furthermore, this circuit requires a very close ratio match between resistor pairs R_1/R_2 and R_3/R_4; otherwise, the gain from each input will be different—directly affecting common-mode rejection. For example, at a gain of 1—with all resistors of equal value—a 0.1% mismatch in just one of the resistors will degrade the CMR to a level of 66 dB (1 part in 2000).

In spite of these problems, this type of "bare bones" IA circuit is useful as a building block within higher performance in-amps. It is also very practical as a stand-alone functional circuit in video and other high speed uses, or in low frequency, high CMV applications, where the input resistors also provide input protection for the amplifier. Monolithic in-amps such as the Analog Devices' AD626 and AMP-03 benefit from their internal pretrimmed resistor networks; both employ variations of the simple subtractor in their design.

Because the circuit divides down the voltage applied to the op-amp, the simple subtractor circuit's input common-mode range can extend beyond that of the op-amp alone. Subtractor resistor matching has been preserved in the AD626 and the AMP-03 designs by using oxide-isolated thin-film resistor networks. As a result, these devices not only reduce cost by providing their own internally trimmed resistors, they are useful in applications where input voltages equal or exceed the supply voltage. For example, when powered by ±15 V supplies, a subtractor can often measure signals with common-mode voltages as high as ±20 volts.

Improving the Simple Subtractor with Input Buffering

An obvious way to significantly improve the subtractor circuit is to add high input impedance buffer amplifiers ahead of the simple subtractor circuit, as shown in the three op-amp instrumentation amplifier circuit of Figure 4.

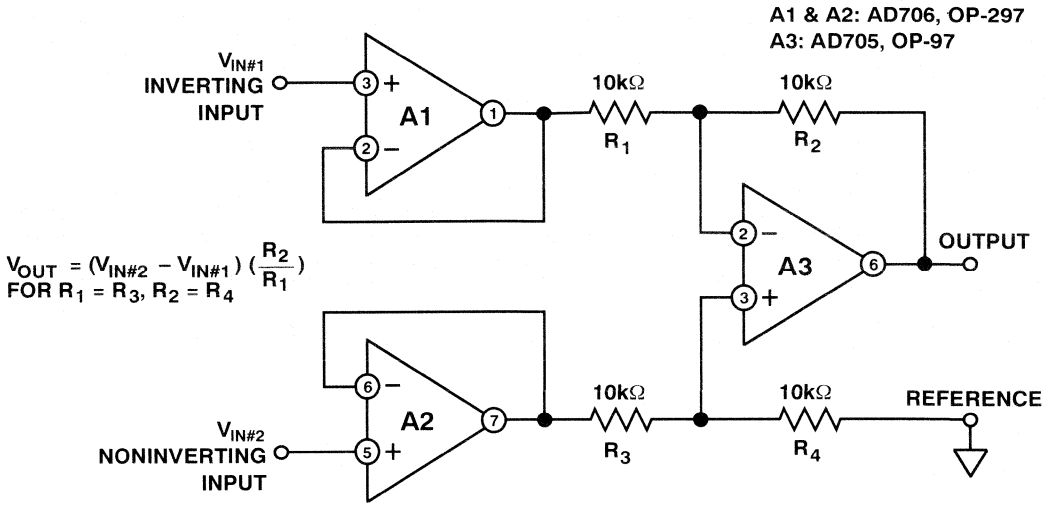


Figure 4. A Subtractor Circuit with Input Buffering

This circuit now provides matched, high impedance inputs so that the impedances of the input sources will have a minimal effect on the circuit's common-mode rejection. The use of a dual op-amp for the two input buffer amplifiers is preferred since they will better track each other over temperature. Although the resistance values are different, this circuit has the same transfer function as the circuit of Figure 3.

Figure 5 shows a further improvement: now the input buffers are operating with gain, which provides a circuit with more flexibility.

If $R_5 = R_8$ and $R_6 = R_7$ and, as before, $R_1 = R_3$ and $R_2 = R_4$, then:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1}) \left(1 + \frac{R_5}{R_6}\right) \left(\frac{R_2}{R_1}\right)$$

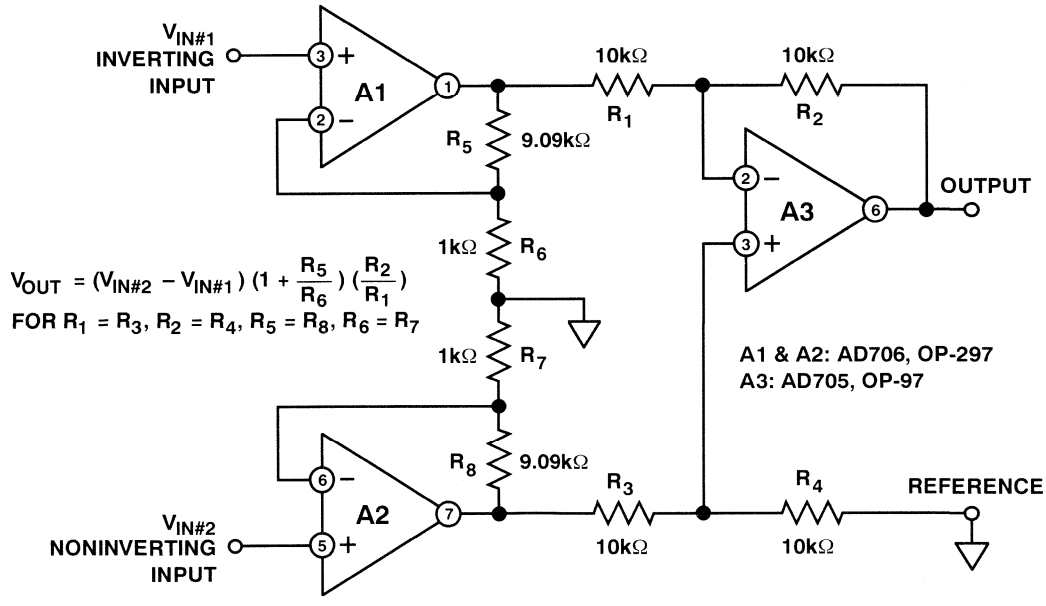


Figure 5. A Buffered Subtractor Circuit Which Has the Buffer Amplifiers Operating with Gain

While the circuit of Figure 5 does increase gain for differential signals, it also increases the common-mode signals. The circuit of Figure 6 provides a final refinement and has become the most popular configuration for instrumentation amplifier design.

The "classic" three op-amp in-amp circuit is a clever modification of the buffered subtractor circuit of Figure 5. In this configuration, a single gain resistor, R_G, connected between the summing junctions of the two input buffers, replaces R_6 and R_7 in the circuit of Figure 5. Now the differential gain may be varied by changing this one external resistor. And once the subtractor circuit has been set up with its ratio-matched resistors, no further resistor matching is required when changing gains. If $R_5 = R_6$ and $R_1 = R_3$ and $R_2 = R_4$, then:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1})\left(1 + \frac{2R_5}{R_G}\right)\left(\frac{R_2}{R_1}\right)$$

As with the previous circuit, op-amps A1 and A2 of Figure 6 buffer the input voltage. Because resistor R_G is connected between the summing junctions of these two amplifiers, the full input voltage will appear across R_G when a differential voltage is applied to the inputs of the in-amp. Since the voltage across R_G equals V_{IN}, the current through R_G will equal: (V_{IN}/R_G). Amplifiers A1 and A2 will, therefore, operate with gain and amplify the input signal. Note, however, that if a common-mode voltage is applied to the amplifier inputs, R_G will then have the same potential on both sides and no current will flow through it. Since no current flows through R_G (and, therefore, through R_5 and R_6), amplifiers

A1 and A2 will operate as unity gain followers. Therefore, common-mode signals will be passed through the input buffers at unity gain, but differential voltages will be amplified by the factor $(1 + (2R_F/R_G))$.

All this means that, in theory at least, the user may take as much gain in the front end as desired (as determined by R_G) without increasing the common-mode gain and error. That is, the differential signal will be increased by gain, but the common-mode error will not, so the ratio (Gain $(V_{DIFF})/(V_{ERROR}$ CM)) will increase. Thus, CMRR will theoretically increase in direct proportion to gain—a very useful property.

Finally, because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. These features explain the popularity of this configuration.

Three Op-Amp In-Amps—Design Considerations

Three op-amp instrumentation amplifiers may be constructed using either FET or bipolar input operational amplifiers. FET input op-amps have very low bias currents and are generally well-suited for use with very high ($>10^6$ Ω) source impedances. FET amplifiers usually have lower CMR, higher offset voltage, and higher offset drift than bipolar amplifiers. They also provide a higher slew rate for a given amount of power. Amplifiers with bipolar

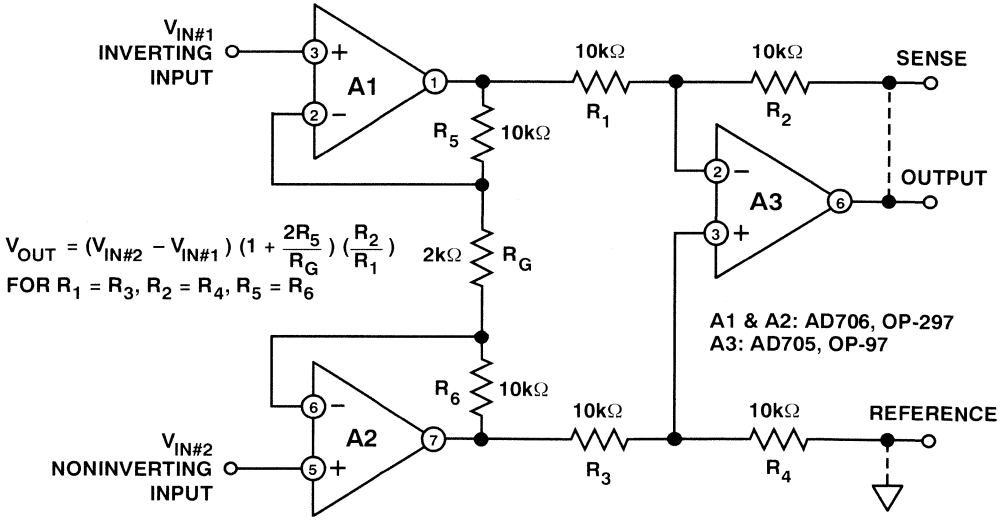


Figure 6. The "Classic" Three Op-Amp In-Amp Circuit

input stages will tend to achieve both higher CMR and lower input offset voltage drift than FET input amplifiers. Superbeta bipolar input stages combine many of the benefits of both FET and bipolar processes, with even lower I_B drift than FET devices.

A common (but frequently overlooked) pitfall for the unwary designer using a three op-amp in-amp design is the reduction of common-mode voltage range which occurs when the in-amp is operating at high gain. Figure 7 is a schematic of a three op-amp in-amp which is operating at a gain of 1000.

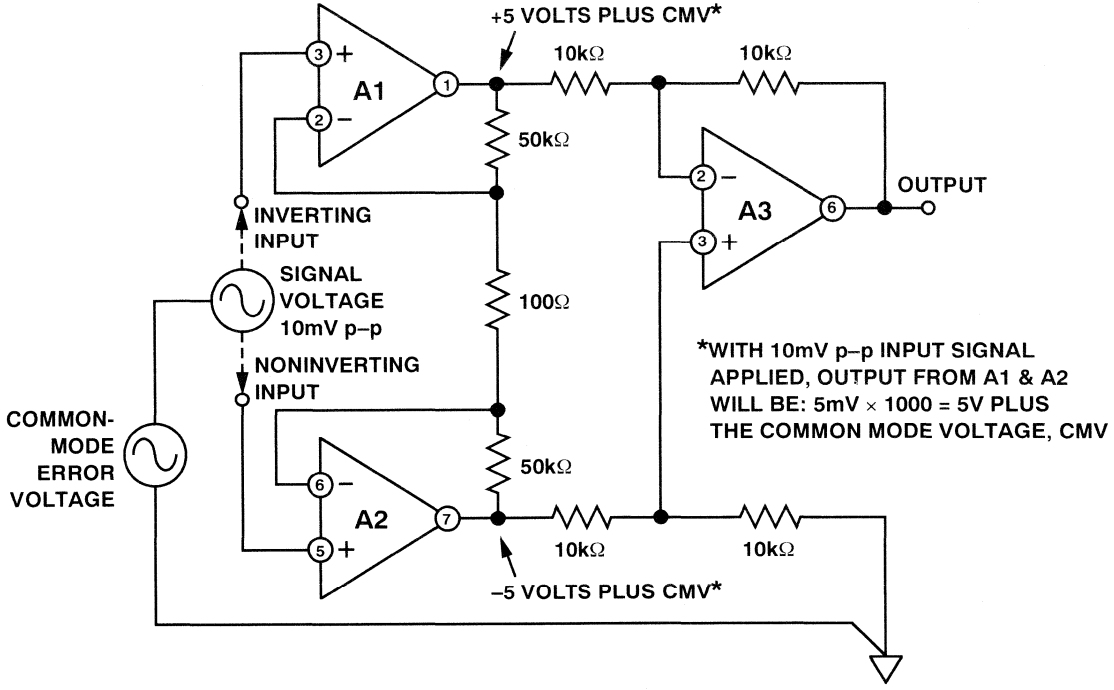


Figure 7. A Three Op-Amp IA Showing Reduced CMV Range

In this example, the input amplifiers, A1 and A2, are operating at a gain of 1000, while the output amplifier is providing unity gain. This means that the voltage at the output of each input amplifier will equal one half the peak to peak input voltage times 1000, plus any common-mode voltage that is present on the inputs (the common-mode voltage will pass through at unity gain regardless of the differential gain). Therefore, if a 10 mV differential signal is applied to the amplifier inputs, then amplifier A1's output will equal +5 volts plus the common-mode voltage and A2's output will be −5 volts plus the common-mode voltage. If the amplifiers are operating from ±15 volt supplies, they will usually have 7 volts or so of headroom left, thus permitting an 8 volt common-mode voltage—but not the full 12 volts of CMV which typically would be available at unity gain. Higher gains, or lower supply voltages, will further reduce the common-mode voltage range.

The Basic Two Op-Amp Instrumentation Amplifier

The two op-amp in-amp approach provides a special class of in-amps: those which are very useful for a few limited applications, but which have serious drawbacks that make them inappropriate for general use.

Figure 8 shows just such a circuit; it has the obvious advantage of requiring only two operational amplifiers, rather than three, with subsequent savings in cost and power consumption. The transfer function of this circuit (without R_G) is:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1}) \left(1 + \frac{R_4}{R_3}\right)$$

$$for\ R_1 = R_4\ and\ R_2 = R_3$$

Input resistance is high, thus permitting the signal source to have an unbalanced output impedance.

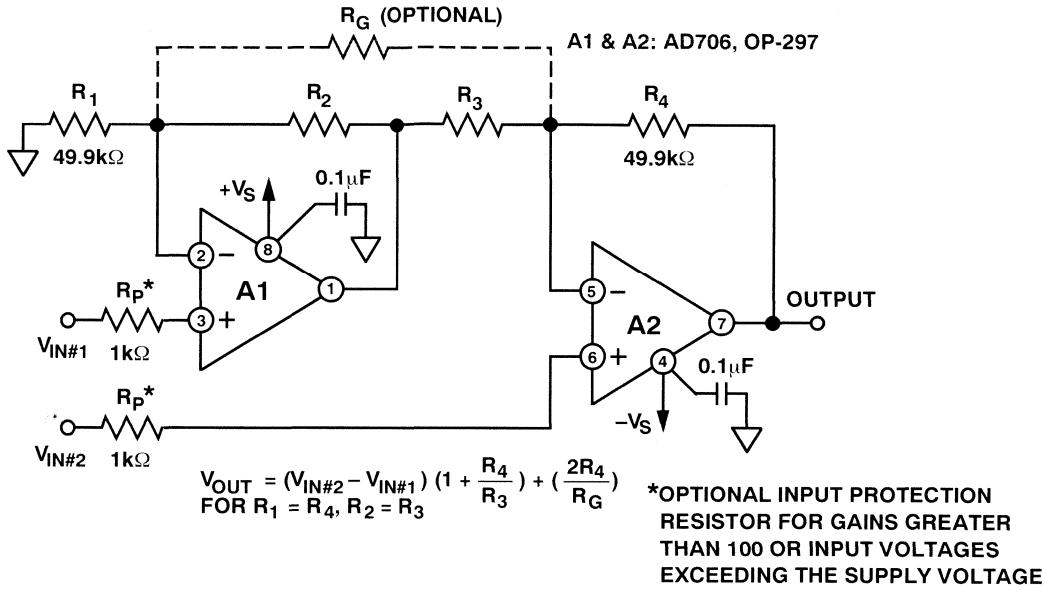


Figure 8. A Two Op-Amp Instrumentation Amplifier

Furthermore, the circuit gain may be fine trimmed using an optional trim resistor, R_G. Like the three op-amp circuit, CMR increases with gain, once initial trimming is accomplished—but CMR is still dependent upon the ratio matching of resistors R_1 through R_4. Resistor values for this circuit using the optional gain resistor, R_G, can be calculated using:

$$R_1 = R_4 = 49.9\ k\Omega$$

$$R_2 = R_3 = \frac{49.9\ k\Omega}{0.9\ G - 1}$$

$$R_G = \frac{99.8\ k\Omega}{0.06\ G}$$

where G = Desired Circuit Gain

Note that, in this configuration, common-mode voltage input range is even more affected by gain than is the three op-amp in-amp circuit, because amplifier A1 amplifies the common-mode voltage by the ratio $1 + (R_2/R_1)$. At high overall circuit gains, amplifier A1 operates at gains very close to unity. But as the overall gain is reduced, A1 operates at increasing gain, greatly reducing its common-mode voltage range. The increasing gain of A1 as overall gain is decreased is shown in Table 1—along with practical 1% resistance values for the circuit of Figure 8. (Note that without resistor R_G, R_2 and R_3 = 49.9 kΩ/G−1.)

Table 1. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 8

Circuit Gain	Gain of A1	Gain of A2	R_2, R_3	R_1, R_4
1.10	11.00	1.10	499 kΩ	49.9 kΩ
1.33	4.01	1.33	150 kΩ	49.9 kΩ
1.50	3.00	1.50	100 kΩ	49.9 kΩ
2.00	2.00	2.00	49.9 kΩ	49.9 kΩ
10.1	1.11	10.10	5.49 kΩ	49.9 kΩ
101.0	1.01	101.0	499 Ω	49.9 kΩ
1001	1.001	1001	49.9 Ω	49.9 kΩ

1 Hz, 4-Pole Low-Pass Filter Recommended Component Values

Desired Low Pass Response	Section 1 Freq (Hz)	Section 1 Q	Section 2 Freq (Hz)	Section 2 Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

Specified values are for a −3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly; i.e., for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, C4 = 0.0205 μF.

In-Amp Section–Recommended Component Values

Circuit Gain	R_1 & R_3	R_G	−3 dB BW
10	6.34 kΩ	166 kΩ	50 kHz
100	526 Ω	16.6 kΩ	5 kHz
1,000	56.2 Ω	1.66 kΩ	0.5 kHz

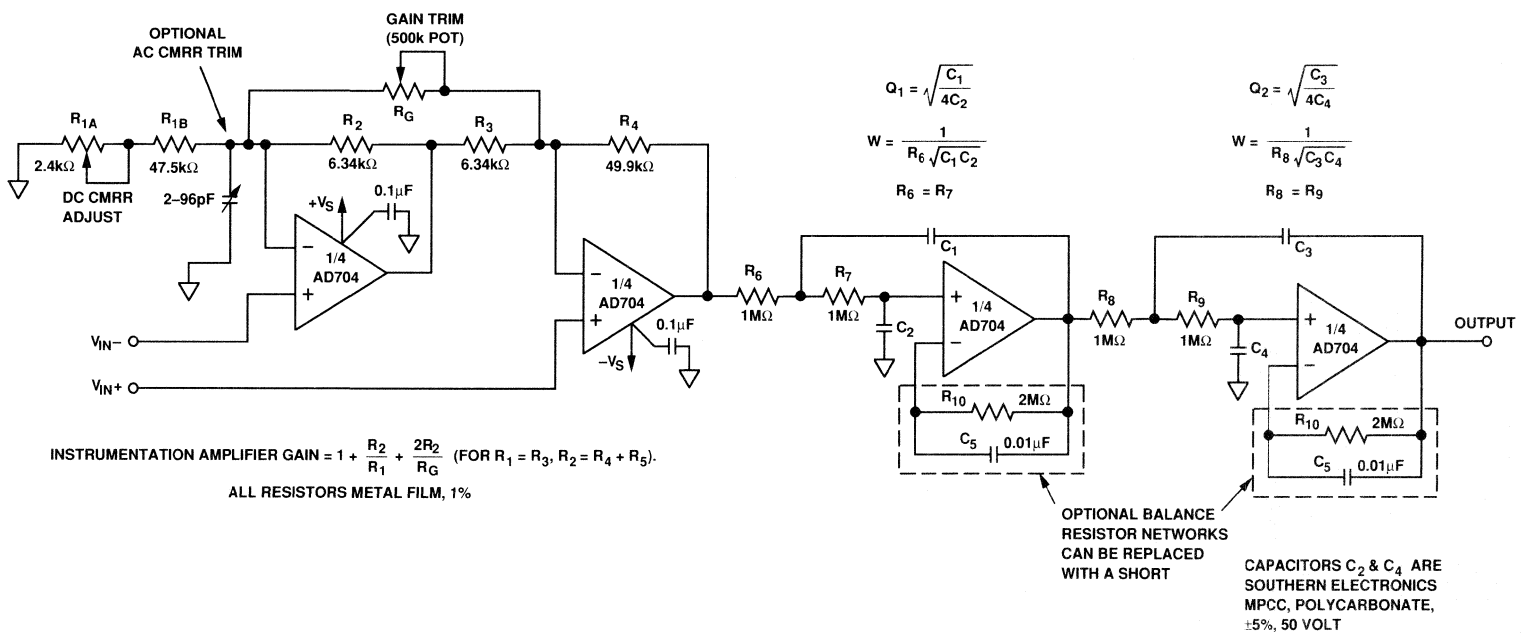


Figure 9. Two Op-Amp In-Amp with Post Filtering

For example, at a gain of 100, the gain of A1 would be 1.01 (i.e., 1 + 0.01), therefore, leaving A1 with 99% of its maximum input voltage range. But, at an overall gain of three (all five resistors equal 49.9 kΩ) amplifier A1 is now operating at a gain of 2 (1 + 1), which will reduce its maximum common-mode range by 50%. These large reductions in input common-mode range at low gains can easily lead to saturation of A1, thus leaving no "head-room" to amplify the differential signal of interest. Also note that the required value of R_2 and R_3 approaches infinity as the circuit gain approaches unity; therefore, this circuit cannot be operated at a gain of one. A final limitation of this circuit is that since the two amplifiers are operating at different closed-loop gains (and thus at different band-widths), there will be generally poor ac common-mode rejection without the use of an ac CMR trim capacitor (connected between Pin 2 of A1 and ground).

A Two Op-Amp IA Circuit with Post Filtering

The circuit of Figure 9 combines a basic two op-amp in-amp circuit with a four-pole post filter to improve performance. Benefits include: a 30 pA input bias current, a 0.2 μV/°C offset voltage drift and only 1.5 mA quiescent current for the entire circuit. Providing a low cost, high gain preamp for transducer applications, it will operate at gains of two or greater. Figure 9 gives component values for a total circuit gain of 10.

The 1 Hz, 4-pole active filter provides high dc precision at low cost while requiring a minimum number of components. The low levels of current noise, input offset and input bias currents in the quad op-amp (either an AD704 or OP-497) allow the use of 1 MΩ resistors without sacrificing the 1 μV/°C drift of the op-amp. Thus lower capacitor values may be used, reducing cost and space. Furthermore, since the input bias current of these op-amps is as low as their input offset currents over most of the MIL temperature range, there rarely is a need to use the normal balancing resistor (along with its noise-reducing bypass capacitor). Note, however, that adding the optional balancing resistor will enhance performance at temperatures above 100°C.

Monolithic Instrumentation Amplifiers

Advantages Over Op-Amp In-Amps

To satisfy the demand for in-amps which would be easier to apply, monolithic IC instrumentation amplifiers were developed. These circuits often incorporate the same design approaches previously used, while providing laser-trimmed resistors and other benefits of monolithic IC technology. Since both active and passive components are now within the same die they can be closely matched—this will insure that the device provides a high CMR. In addition, these components will stay matched over temperature, assuring excellent performance over a wide temperature range. IC technologies such as laser wafer trimming allow monolithic integrated circuits to be "tuned-up" to very high accuracy and provide low cost, high volume manufacturing.

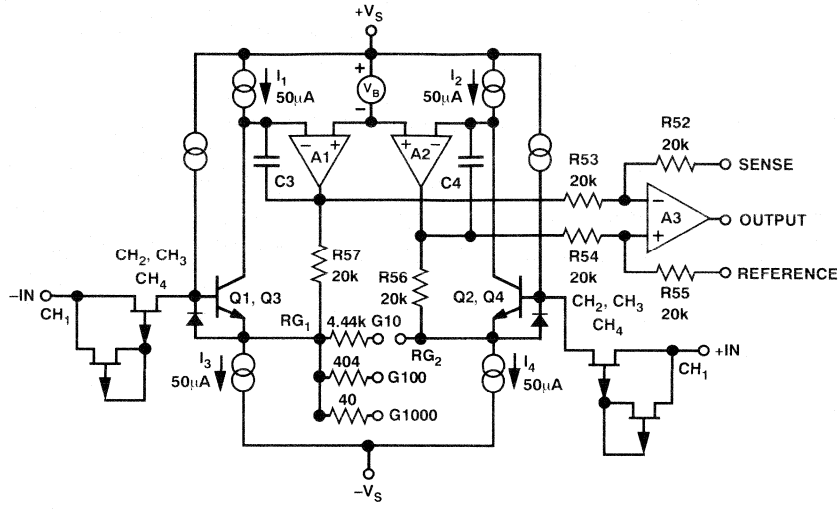


Figure 10. A Simplified Schematic of the AD524 Monolithic Instrumentation Amplifier

Monolithic In-Amp Design—The Inside Story

The AD524 is a good example of current monolithic instrumentation amplifier design. It is based on the classic three op-amp in-amp circuit previously described. The AD524 simplified schematic is shown in Figure 10. Note that the AD620 and AMP-02 both use a similar circuit architecture and offer many of the same performance benefits.

In these designs, the desired gain is selected by varying the value of external resistor R_G. Feedback forces the collector currents of Q1, Q2, Q3, and Q4 to be constant which impresses the input voltage across R_G. As R_G is reduced, thus increasing the programmed gain, the transconductance of the input preamp increases until it equals the transconductance of the input transistors.

The AD524 achieves a very high open-loop gain of 3×10^8 while operating at a programmed closed-loop gain of 1000. This reduces gain related errors to 30 ppm. It also features a high gain/bandwidth product of 25 MHz, determined by capacitors C3 and C4 and the input transconductance. Additionally, the AD524 is a very low noise in-amp—with only 7 nV/$\sqrt{\text{Hz}}$ noise @ at gain of 1000.

The AD524 has its own internal input protection. As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overload, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, (10 or less) the gain resistor acts as a current-limiting element in series with the inputs. At high-gains, the lower value for R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place a limiting resistor in series with each input. But limiting input current below 5 mA, with the full differential overload of 36 volts applied, requires over 7 kΩ of resistance. This added resistance will increase noise by 10 nV$\sqrt{\text{Hz}}$. Unfortunately, using a normal FET device will allow the input to go negative with respect to the drain, causing the gate-drain junction to be forward biased (Figure 11a). The FET then acts as a large-area diode, with forward current increasing exponentially with applied voltage.

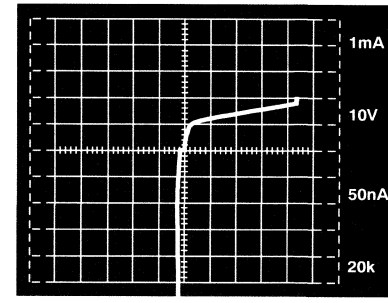


Figure 11a. V/I Characteristics of FET with Gate Shorted to Source. 1 mA per Vertical Division, 10 Volts per Horizontal Division.

Therefore, to overcome this problem, a special series protection FET was used in the AD524 to provide both input protection and low noise. The

schematic representation of this device (Figure 11b) illustrates the interconnection of the FET electrodes. Figure 11c is a curve-tracer plot of the V/I characteristics of this FET circuit that clearly illustrates bidirectional current-limiting ability.

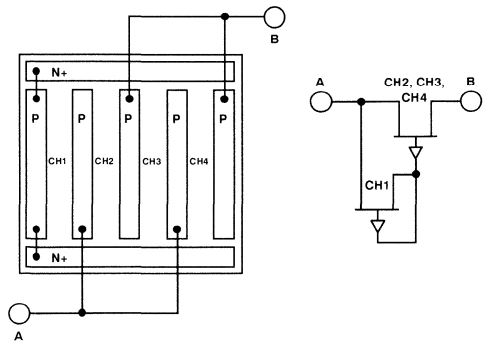


Figure 11b. Bidirectional Current Limit FET and Its Schematic Representation

This protects the in-amp from both positive and negative input overloads. Under nonoverload conditions, the three channels, CH2, CH3, CH4, act as an ≈1 kΩ resistance in series with the input. During an overload in the positive direction, the fourth channel, CH1, acts as a small resistance (≈3 kΩ) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH1; and when this FET goes into saturation, the

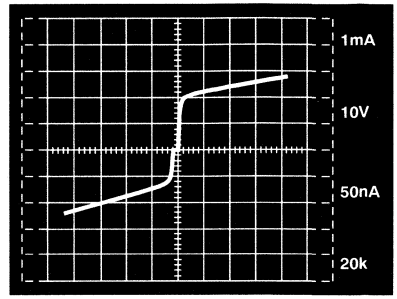


Figure 11c. V/I Characteristics of Bidirectional Current Limit FET. 1 mA per Vertical Division, 10 Volts per Horizontal Division.

gate current is limited and the main FET will go into a controlled enhancement. This bidirectional limiting holds the maximum input current to 3 mA at the maximum overload voltage of 36 volts .

The AMP-01, another monolithic in-amp, incorporates a unique current feedback architecture into its design, achieving both a very high common-mode rejection and a relatively constant bandwidth over a wide range of gains. A simplified schematic of the AMP-01 is shown in Figure 12.

Amplifier gain may be set between 0.1 to 10,000 and is determined by the ratio of two resistors, R_{SCALE} (R_S) and R_{GAIN} (R_G) according to the expression:

$$Gain = \frac{20\ R_{SCALE}}{R_{GAIN}}$$

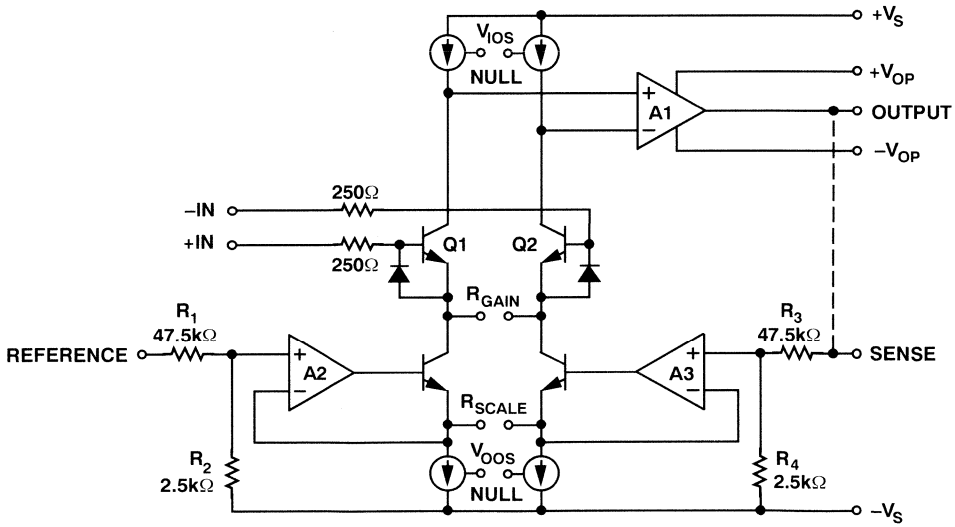


Figure 12. A Simplified Schematic of the AMP-01 Monolithic In-Amp

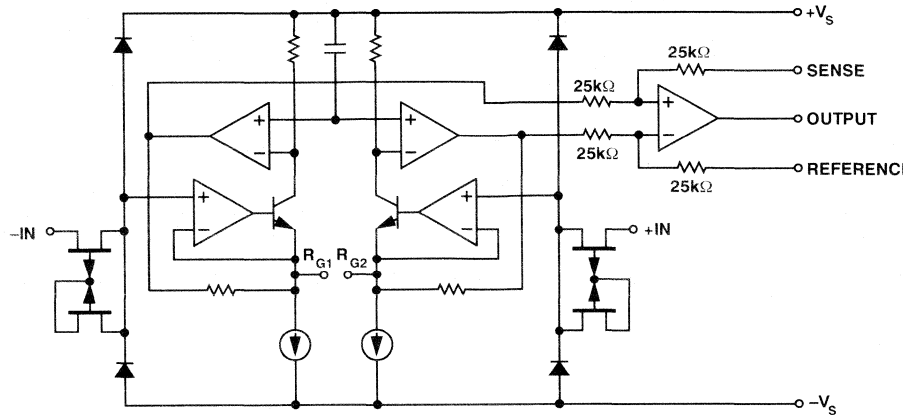


Figure 13a. A Simplified Schematic of the AMP-02 Monolithic In-Amp

The overall amplifier gain temperature coefficient is better than 15 ppm/°C when the temperature coefficient of resistors R_S and R_G is matched to 5 ppm/°C or better.

Referring to the simplified schematic, the current feedback works as follows. As voltage is applied across the inputs of the AMP-01, that same voltage develops across resistor R_{GAIN} which steers current from one leg of the differential stage to the other. This causes the output amplifier to swing, feeding signal back via the sense pin, which converts a fraction of that signal into a current that steers the current flowing in R_{GAIN} into R_{SCALE}—but in the reverse direction, to equalize the imbalance. This current feedback scheme results in a common-mode rejection better than 120 dB over a wide temperature range. This design exhibits a constant 50 kHz bandwidth within a gain range of 1 to 100. Additionally, the amplifier can settle in 15 μs to 0.01% accuracy, independent of gain thus allowing high speed data acquisition with a high throughput rate.

Additionally, the (high) combined gains of the input and output stages result in excellent linearity and gain accuracy—to 16-bit performance at a gain of 1000.

The AMP-01 is laser trimmed to yield low input offset voltage and high CMR. In addition, its input stage uses ion-implanted superbeta transistors together with a bias-current-cancellation circuit to reduce input bias current to less than 10 nA over the −40°C to +85 °C temperature range.

A third member of the Analog Devices' family of "rugged-ized" instrumentation amplifiers is *the AMP-02*. Similar to the AD524, it also employs a series input FET protection scheme, as shown in Figure 13a. This protection circuit limits the input current to ±4 mA and prevents damage to the inputs with differential overloads as high as 60 V.

Figure 13b shows the input current limiting action as the input overload voltage increases. Note that the protection is still active with, or without, power applied. In addition to current limiting, this design uses a pair of internal diodes to clamp the inputs to the power supply rails, when either input is exposed to a voltage higher than that of the supply. This effectively prevents damage due to input stage breakdown.

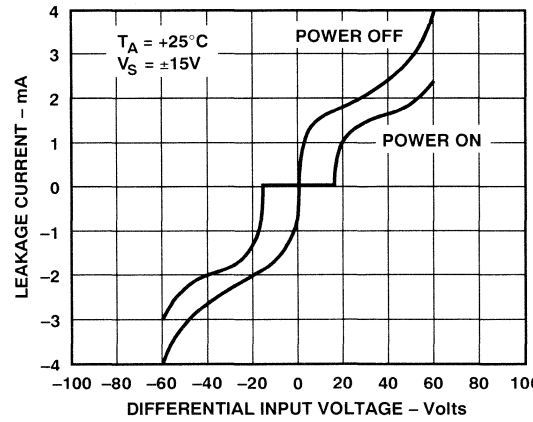


Figure 13b. The Overload Characteristics of the AMP-02

The AD620 is a monolithic instrumentation amplifier which provides a low cost, low power in-amp function in an 8-pin SOIC package. Gain is programmed using a single external resistor. By design, the required resistor values for gains of 10 and 100 are standard 1% metal film resistor values.

The design is another modification of the classic three op-amp approach. Absolute value trimming allows the user to program the desired gain accuracy—to 0.5% max at a gain of 100, using only one external resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components.

A preamp section comprised of Q1 and Q2 provides additional gain up front. Feedback through the Q1–A1–R1 loop and the Q2–A2–R2 loop maintains a constant collector current through the input devices Q1, Q2, thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2)/R_G + 1. The unity gain subtractor A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: First, the open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors. Next, the gain bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing the amplifier's frequency response. Finally, the input voltage noise is reduced to a value of 9 nV/$\sqrt{\text{Hz}}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2 are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor. The gain equation is then:

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that:

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

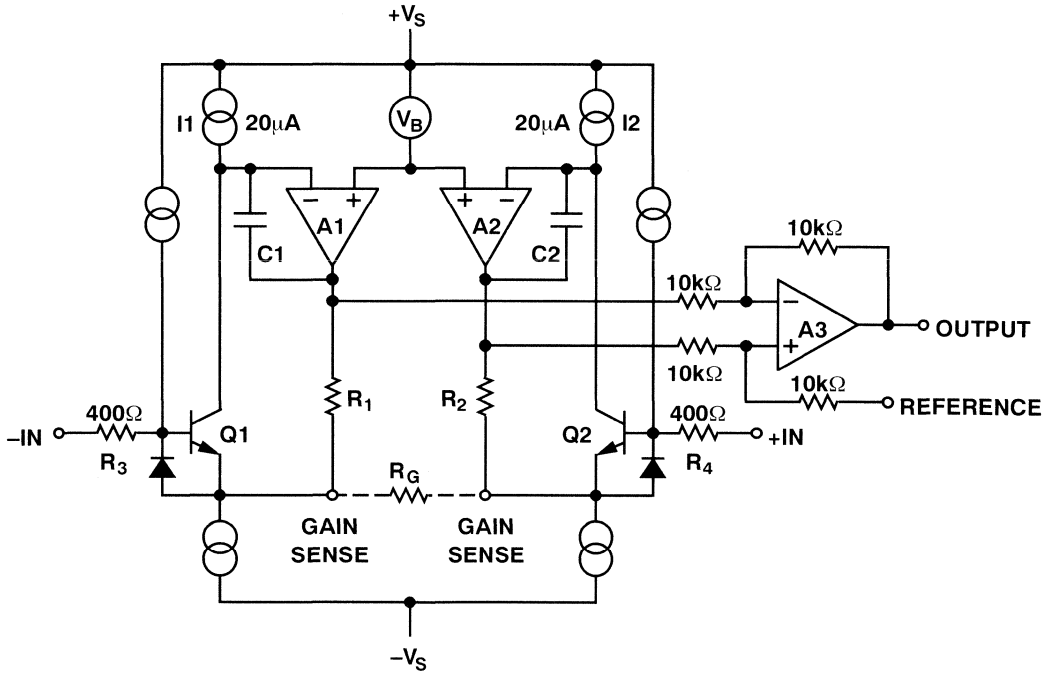


Figure 14. A Simplified Schematic of the AD620

The AD621 is similar to the AD620, except that for gains of 10 & 100, the gain setting resistors are on the die—no external resistors are used. This provides excellent gain stability over temperature. The AD621 also has superior gain nonlinearity over that of the AD620. The AD621 may also be operated at gains between 10 and 100 by using an external gain resistor although gain error and gain drift over temperature will be degraded. Figure 15 is a simplified schematic of the AD621.

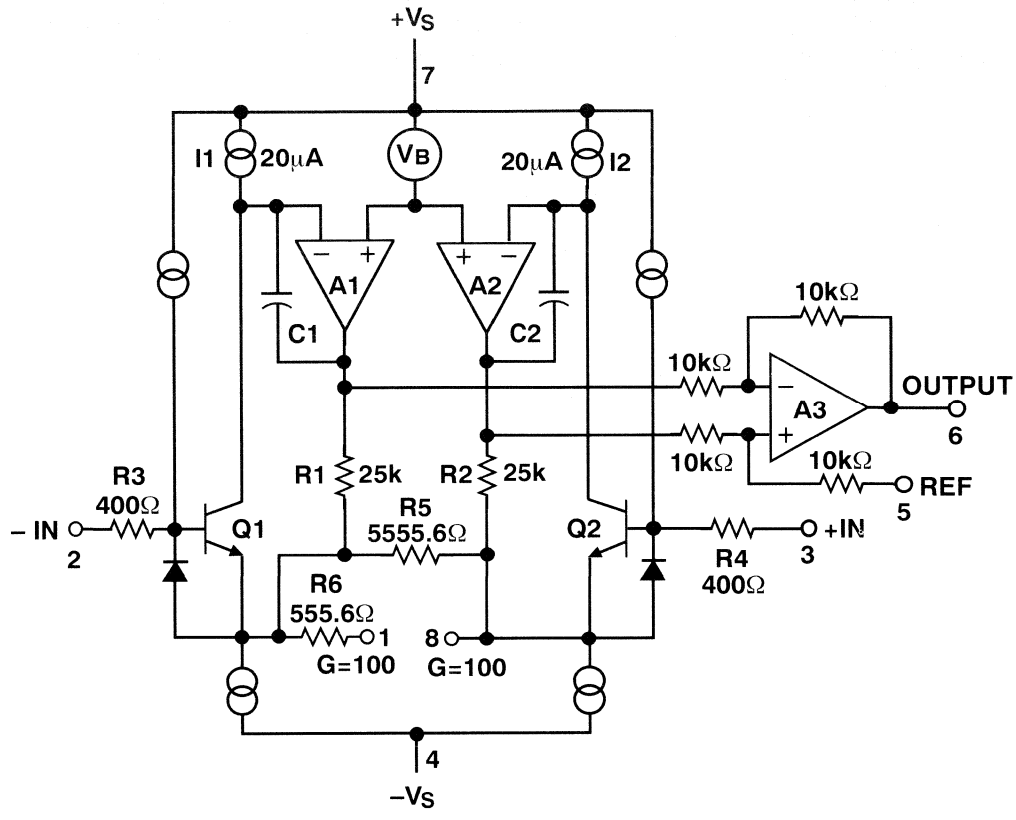


Figure 15. A Simplified Schematic of the AD621

Monolithic In-Amps Optimized for High Performance

The AD624, is a monolithic in-amp similar to the AD524, but optimized for even higher accuracy and lower noise. Figure 16 is a simplified schematic of the AD624.

The gain equation for this circuit is:

$$Gain = \frac{40{,}000\ \Omega}{R_G} + 1$$

Note that the chief differences between the AD524 and AD624 circuits are in their input sections and their internal scaling resistors, allowing the AD624 to provide different preset gains than those of the AD524. For details concerning the entire line of monolithic in-amps produced by Analog Devices, refer to Appendix B.

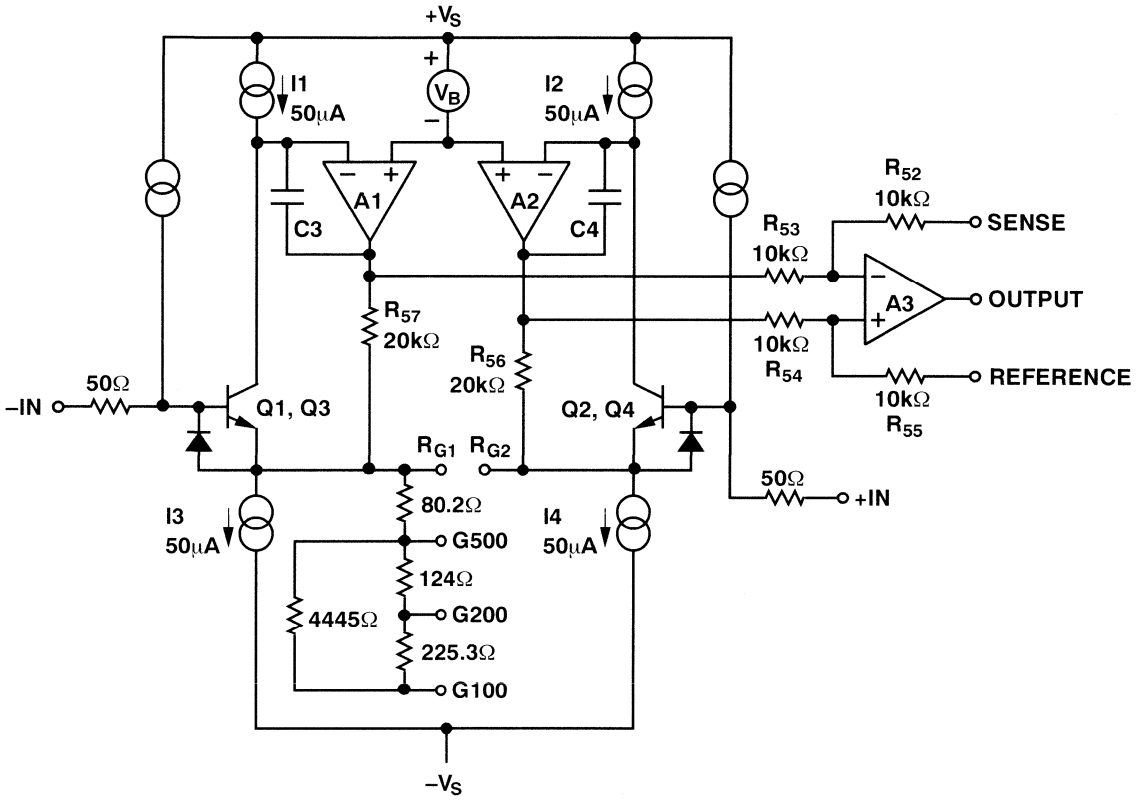


Figure 16. AD624 Simplified Schematic

In-Amps Optimized for Single Supply Operation

The AD626 is a single or dual supply differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (V_{CM}), without the use of any other active components.

Figure 17 shows the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators R1 through R4 whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op-amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages—six times greater than that which can be tolerated by the actual input to A1. As a result, the input common-mode range extends to six times the quantity (V_S − 1 V). The overall common-mode error is minimized by precise laser-trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio (CMRR) of at least 10,000:1 (80 dB).

The output of A1 is connected to the input of A2 via a 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest.

The AD626 is easily configured for gains of 10 or 100. For a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded.

Gains between 10 and 100 are easily set by connecting a resistor between Pin 7 and Analog GND. Because the on-chip resistors have an absolute tolerance of ±20% (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The nominal value for this gain setting resistor is equal to:

$$R = \frac{50{,}000\ \Omega}{Gain - 10} - 555\ \Omega$$

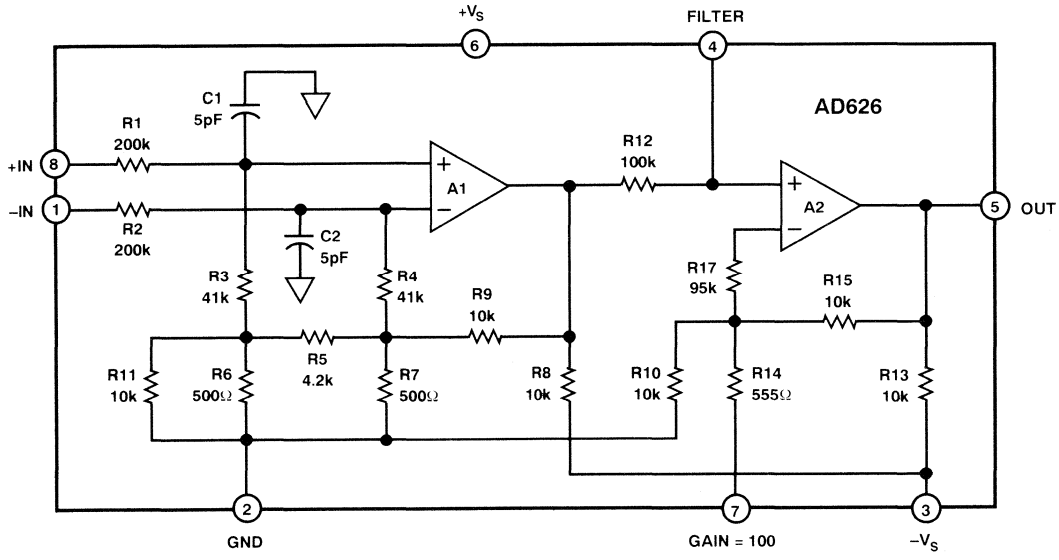


Figure 17. AD626 Simplified Schematic

The AMP-04 is another low power, single-supply instrumentation amplifier. Its excellent combination of impressive specifications and single supply capability offers designers performance difficult to match with discrete components.

It is a true instrumentation amplifier with high impedance inputs and common-mode rejection ratios in excess of 85 dB. Gains of 1 to 1000 are set by a single external resistor to an accuracy of better than 0.5%. Input offset voltage is below 200 μV. Noise is typically a low 10 nV/$\sqrt{\text{Hz}}$ at a gain of 1000, and the user access at Pins 6 and 8 permits easy bandwidth limiting of the amplifier for improved noise performance.

Figure 18 is a block diagram of the AMP-04.

In addition to the high impedance inputs, a reference input is available for offsetting the output. This feature is very useful in single supply systems which have input signals that represent values of greater and less than zero. Common applications for this are in temperature measurements that are above and below freezing and for pressure sensors that can monitor both vacuum and pressure. Input signal range includes ground and goes to within 1.5 volts of the positive supply.

The AMP-04 consumes only 550 μA of power and can operate from supplies ranging from +4.5 volts to ±18 volts. It offers an excellent combination of speed, accuracy and ease-of-use. It is available in both 8-pin DIP and SOIC packages.

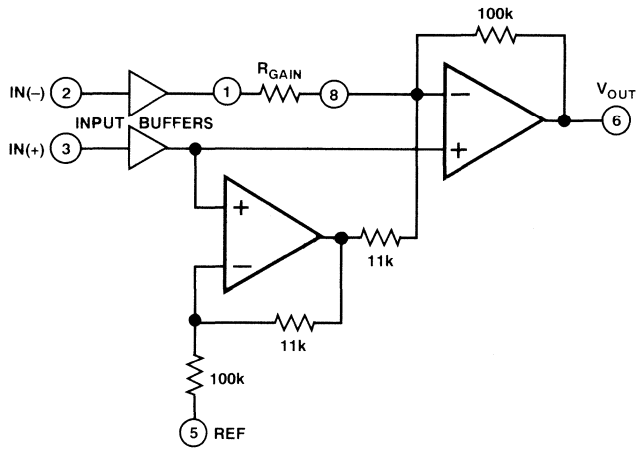


Figure 18. A Block Diagram of the AMP-04

External CMR and Settling Time Adjustments

One of the virtues of the three amplifier in-amp design is that it may be readily "tuned-up" for best performance by external trimming. The dc CMR should always be trimmed first, since it affects CMRR at all frequencies. The $+V_{IN}$ and $-V_{IN}$ terminals should be tied together and a dc input voltage applied between the two inputs and ground. The voltage should be adjusted to provide a 10 volt dc input. A dc CMR trimming potentiometer is then adjusted (as shown in Figure 23) so that the outputs are equal, and as low as possible, with both a positive and a negative dc voltage applied.

AC CMR trimming (Figure 23) is accomplished in a similar manner, except that this time an ac input signal is applied. The input frequency used should be somewhat lower than the −3 dB bandwidth of the circuit. The input amplitude should be set at 20 volts peak-to-peak with the inputs tied together. The ac CMR trimmer is then nulled—set to provide the lowest output possible. If the best possible settling time is needed, the ac CMR trimmer may be used, while observing the output waveform on an oscilloscope. Note that, in some cases, there will be a compromise between the best CMR and the fastest settling time.

RTI and RTO Errors

A second consideration is how circuit gain affects many in-amp error sources. An in-amp should be regarded as a two section amplifier with an input and an output section. Because the errors of the output section are multiplied by a fixed gain (usually one), this section is the principle error source at low circuit gains. As the overall gain is increased, any errors contributed by the input section are multiplied directly and thereby become dominant. All input-related specifications are classified as "referred to input" (RTI) errors while all output-related specifications are considered "referred to output" (RTO) errors.

By separating these errors, it is possible to evaluate the total error, independent of the selected gain setting. For a given gain, an in-amp's input and output errors can be combined to provide a total error specification which is either referred to the input (RTI) or to the output (RTO) by using the following formulas:

Total Error, RTI =
Input Error + (Output Error/Gain)

Total Error, RTO =
(Gain × Input Error) + Output Error

As an example, a typical AD524 will have a +250 μV output offset error and a −50 μV input offset error. In a unity gain configuration, the total offset RTO would be +200 μV, which is the sum of the two. Note that for unity gain, the total offset is the same RTO or RTI. At a gain of 100, the combined offset RTO would be 100 (−50 μV) +250 μV which equals − 4,750 μV or −4.75 mV. The combined offset RTI at a gain of 100 would equal: −50 μV +(250 μV/100) = −47.5 μV.

Cable Termination

When in-amps are used at frequencies above a few hundred kilohertz, properly terminated 50 or 75 ohm coaxial cable should be used for input and output connections. Normally, cable termination is simply a 50 or 75 ohm resistor connected between the cable center conductor and its shield at the end of the coax cable. Note that a buffer amplifier may be required to drive these loads to useful levels.

Power Supply Bypassing, Active Decoupling and In-Amp Stability Issues

Power supply decoupling is an important detail which is often overlooked by designers. Normally, bypass capacitors (values of 0.1 μF are typical) are connected between the power supply pins of each IC and ground. While usually adequate, this practice can be ineffective or even create worse transients than no bypassing at all. It is important to consider where the circuit's currents originate, where they will return, and by what path. Then, once that has been established, bypass these currents around ground and other signal paths. In general, most monolithic in-amps have their integrators referenced to the negative supply (such as the AD524, AD624, AD625, and AD620) and should be decoupled with respect to the output reference terminal. This means that, for each chip, a bypass capacitor should be connected between

each power supply pin and the point on the board where the in-amp's reference terminal is connected. For a much more comprehensive discussion of these issues refer to the application note: "An I.C. Amplifier Users' Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by Paul Brokaw, available free from Analog Devices.

Data Acquisition

Transducer Interface Applications

Instrumentation amplifiers have long been used as preamplifiers in transducer applications. High quality transducers typically provide a highly linear output but at a very low level and a characteristically high output impedance. This requires the use of a high gain buffer/preamplifier which will not contribute any discernible noise of its own to that of the signal. Furthermore, the high output impedance of the typical transducer may require that the in-amp have a low input bias current.

Table 2 gives typical characteristics for some common transducer types.

Since most transducers are slow, bandwidth requirements of the in-amp are modest: a 1 MHz small signal bandwidth at unity gain is quite adequate for most applications.

Table 2. Typical Transducer Characteristics

Transducer Type	Type of Output	Output Impedance	Recommended ADI In-Amp
Thermistor	Resistance Changes with Temperature	50 Ω to 1 MΩ @ +25°C	AD524 AD620, AD621 AMP-01 AMP-02
Type "J" Thermocouple Iron (+) Constantan	Variable Voltage 10 to 100 μV/°C	20 Ω to 2 kΩ	AD624 AD620, AD621 AMP-01
Resistance Temperature Detector (RTD) (In Bridge Circuit)	Resistance Changes with Temperature 0.1%/°C to 0.66%/°C	20 Ω to 20 kΩ @ 0°C	AD624 AD620, AD621 AD625 AMP-01
Level Sensors Thermal Types Float Types	 Variable Resistance Variable Resistance	 500 Ω to 2 kΩ 100 Ω to 2 kΩ	 AD626 AMP-01 AMP-02 AMP-04
Load Cell (Strain Gage Bridge) (Weight Measurement)	Variable Resistance 2 mV/V of Excitation Full Scale	120 Ω to 1 kΩ	AD624 AD620, AD621 AD625, AD626 AMP-01 AMP-02
Photodiode Sensor	Current Increases with Light Intensity. 1 pA – 1 μA I_{OUTPUT}	10^9 Ω	AMP-05
Hall-Effect Magnetic Field Sensors	5 mV/kG-120 mV/kG	1 Ω to 1 kΩ	AD621 AD624 AD620 AD625 AMP-02
Accelerometer	1 to 100 mV/"g"	500 Ω	AD624 AD620, AD621 AD625 AMP-02

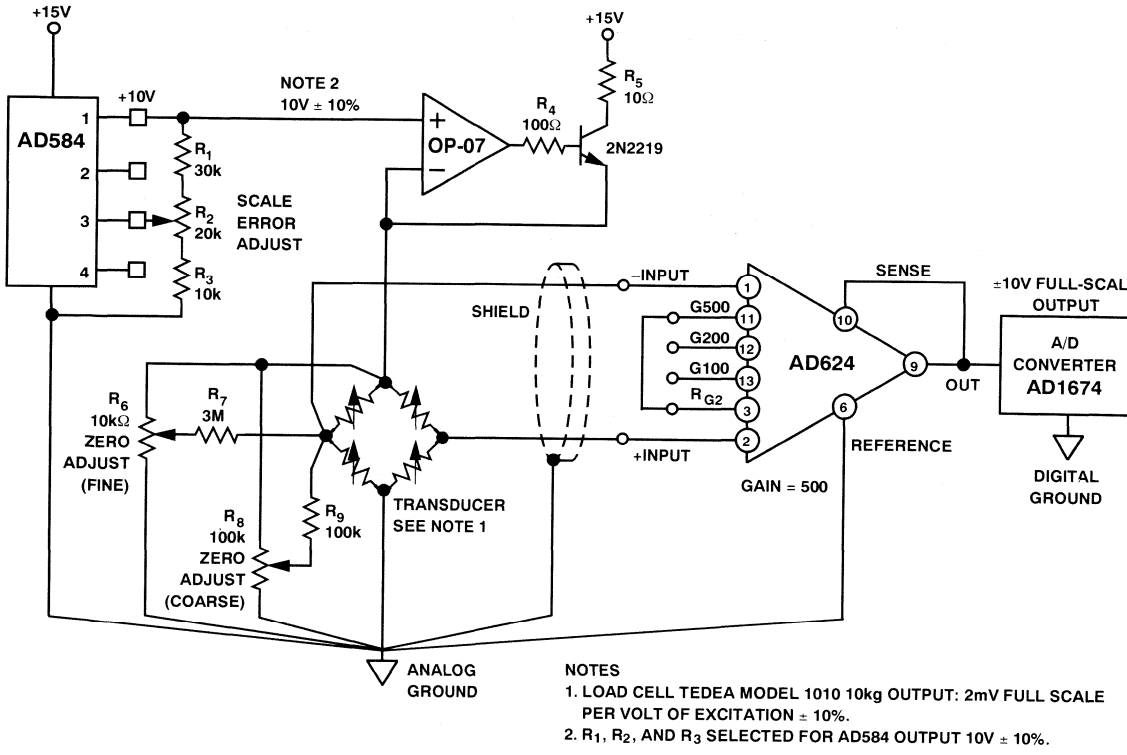


Figure 19. An In-Amp Used in a Weigh Scale Application

Bridge Applications

Instrumentation amplifiers are widely used for buffering and amplifying the small voltage output from transducers which make use of the classic four resistor Wheatstone bridge.

Figure 19 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type, particularly where it is desirable to measure small changes in weight as compared to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offset and gain errors, and offset drifts thus making true 14-bit performance possible.

A Software Programmable Gain Amplifier (SPGA)

An SPGA provides the ability to externally program precision gains from digital inputs. Historically, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drift over temperature. The AD625 monolithic instrumentation amplifier eliminates this problem by making gain "drive" and gain "sense" pins available (Pins 2, 15, 5, 12). This allows the multiplexer's "ON" resistance to be removed from the signal current path, thereby transforming the "ON" resistance error into a small nullable offset error.

Figure 20 shows an SPGA using the AD625. Gains of 1, 4, and 64 may be selected. With the switches set as shown, resistance R_G equals the resistance between the gain sense lines (Pins 2 and 15) of the AD625; therefore, R_G equals the sum of the two 975 Ω resistors and a 650 Ω resistor which together equal 2600 Ω. Therefore, R_F equals the resistance between the gain sense and the gain drive pins (Pins 12 and 15, or Pins 2 and 5), that is, R_F equals the 15.6 kΩ resistor plus the 3.9 kΩ resistor which equals 19.5 kΩ.

The circuit gain, therefore, equals:

$$\frac{2\,R_F}{R_G} + 1 = \frac{2\,(19.5\,k\Omega)}{(2.6\,\Omega)} + 1 = 16$$

As the other switches of the differential multiplexer close synchronously, R_G and R_F change, resulting in other programmed gain settings.

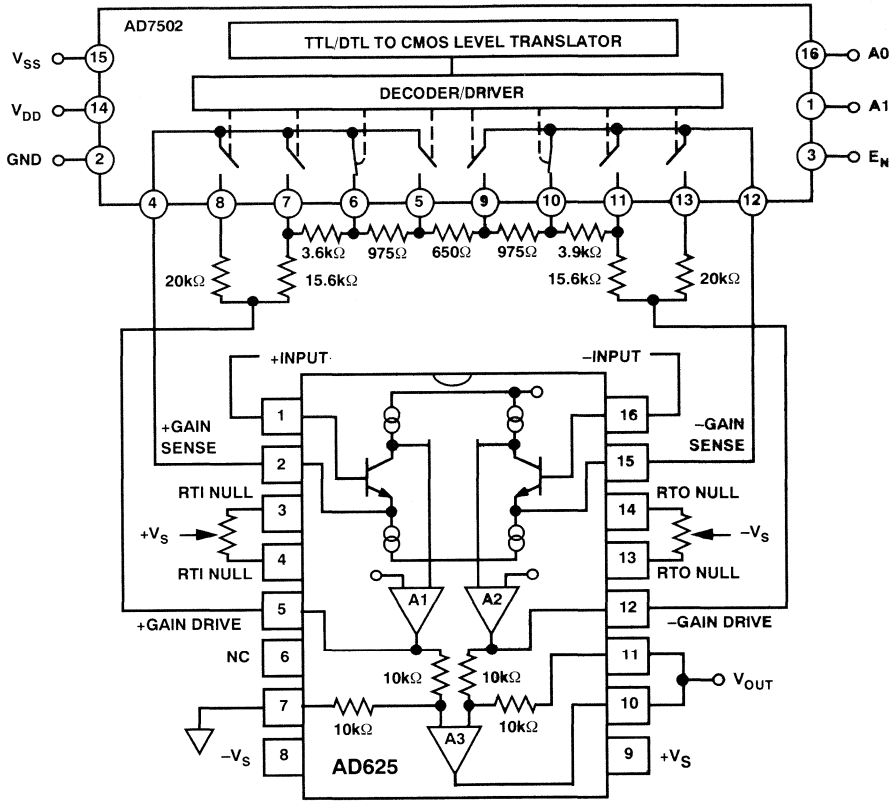


Figure 20. A Software Programmable Gain Amplifier

A High Performance In-Amp Circuit for Data Acquisition

The circuit of Figure 21 has a 3 dB bandwidth of 4 MHz at a gain of 1 and 750 kHz at a gain of 10 and provides a range of gains from unity to over 1000. Settling time for the entire circuit (at a gain of 10) is less than 2 μs to within 0.01% for a 10 volt step, which makes it appropriate for buffering medium speed ADCs (up to 500 kHz) such as the AD678.

Gain	R_G	Bandwidth	t_{SETTLE} (0.01%)
2	20 kΩ	2.5 MHz	1.0 μs
10	4.04 kΩ	1 MHz	2.0 μs
100	404 Ω	290 kHz	5.0 μs

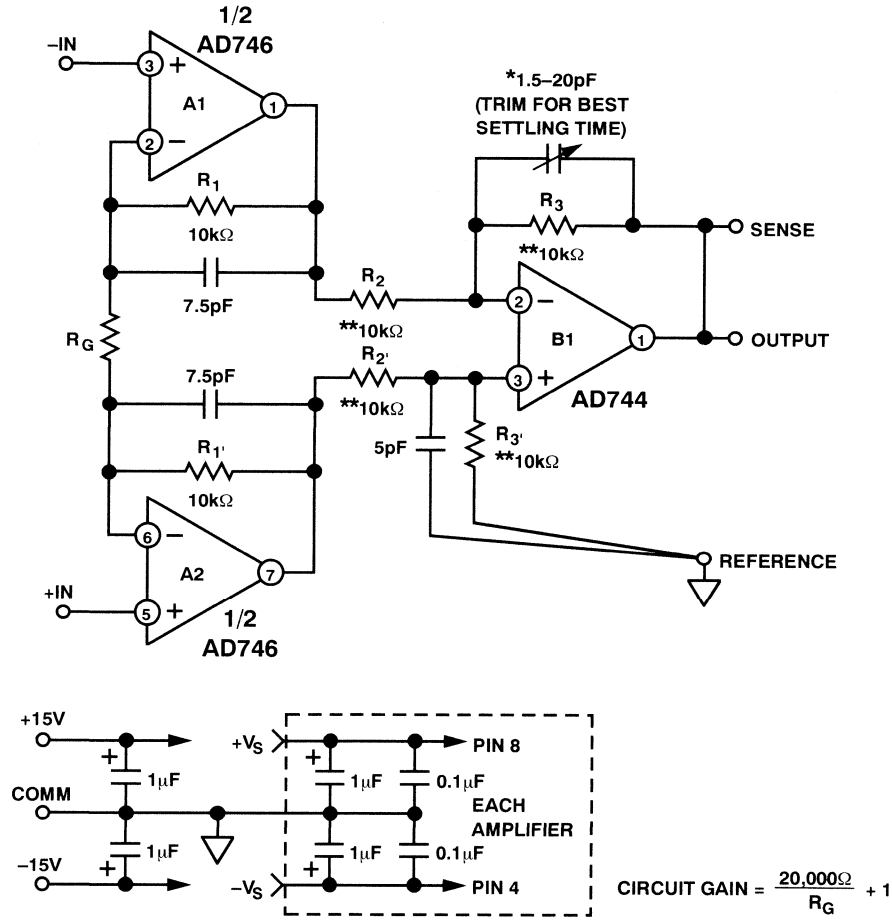


Figure 21. A High Performance, Medium Speed In-Amp Circuit for Data Acquisition

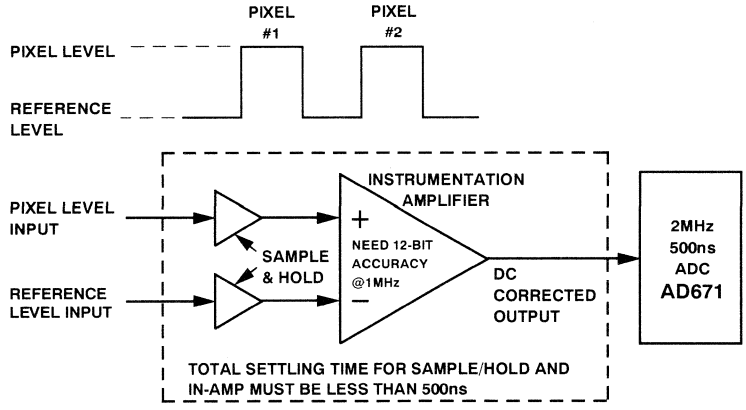
High Speed Data Acquisition

As the speed and accuracy of modern data acquisition systems has increased, there has developed a growing need for high bandwidth instrumentation amplifiers—particularly in the field of CCD imaging equipment where offset correction and input buffering are required. Here double-correlated sampling techniques are often used for offset correction of the CCD imager. As shown in Figure 22a, two sample-and-hold amplifiers monitor the pixel and reference levels and a dc corrected output is provided by feeding their signals into an instrumentation amplifier.

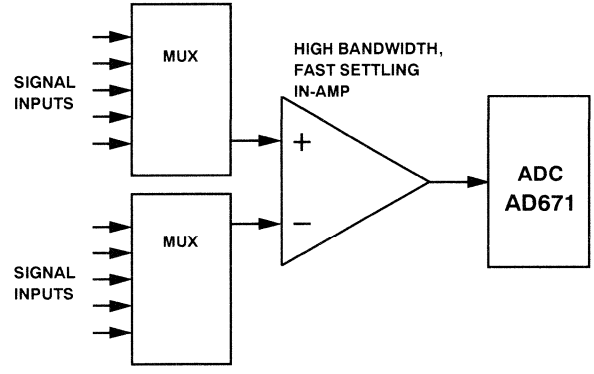
Figure 22b shows how a single multiplexed high bandwidth in-amp can replace several slow speed nonmultiplexed buffers. The system benefits from the common-mode noise reduction, and subsequent increase in dynamic range which the in-amp provides.

Previously, the low bandwidths of commonly available instrumentation amplifiers, plus their inability to drive 50 Ω loads has restricted their use to low frequency applications—generally below 1 MHz. Some higher bandwidth amplifiers have been available, but these have been fixed gain types with internal resistors. With these amplifiers, there was no access to the inverting and noninverting terminals of the amplifier. Using modern op-amps, employing the complementary bipolar or "CB" process, video bandwidth instrumentation amplifiers may now be constructed which offer both high bandwidths and impressive dc specifications. Common-mode rejection may be optimized by trimming or by using low cost resistor arrays.

The bandwidth and settling time requirements demanded of an in-amp buffering an ADC and for the sample-and-hold function preceding it can be quite severe. The input buffer must pass the signal



a. In-Amp Buffers ADC and Provides DC Correction



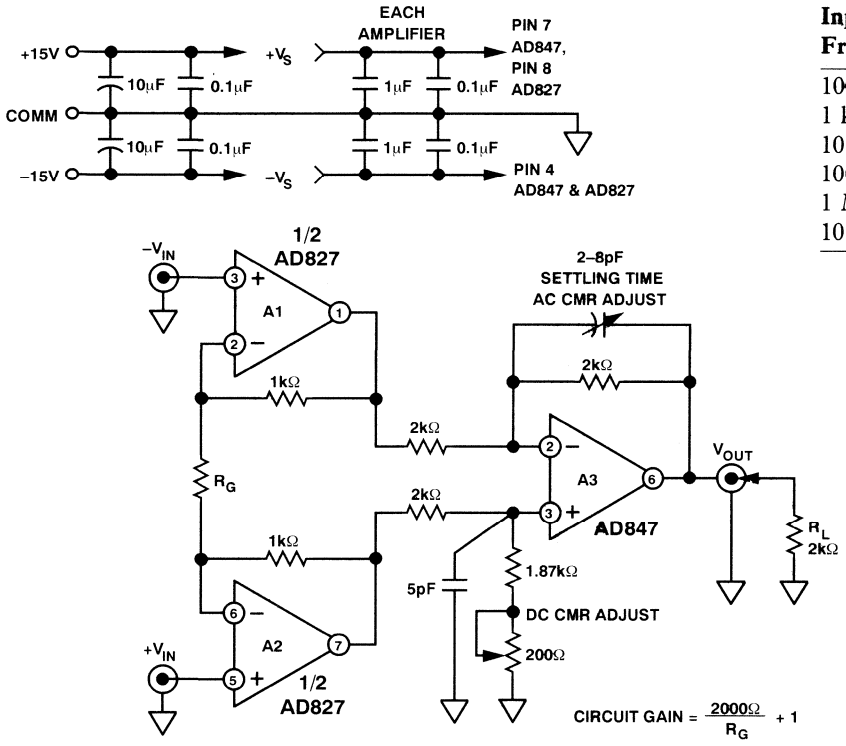
b. Single High Speed In-Amp and Mux Replace Several Slow Speed Buffers

Figure 22. Typical Applications of High Bandwidth In-Amps Buffering ADCs

along fast enough so that the signal is fully settled before the ADC takes its next sample. At least two samples per cycle are required for an ADC to unambitiously process an input signal ($F_S/2$)—this is referred to as the "Nyquist criteria." Therefore, a 2 MHz ADC, such as the AD671, requires that the input buffer/sample hold sections preceding it provide 12-bit accuracy at a 1 MHz bandwidth. Settling time is equally important: the sampling rate of an ADC is the inverse of its sampling frequency—for the 2 MHz ADC, the sampling rate is 500 ns. This means that, for a total throughput rate of less than 1 μs, these same input buffer/sample hold sections must have a total settling time of less than 500 ns.

A High Speed, Three Op-Amp In-Amp

The circuit of Figure 23 lends itself well to CCD imaging and other video speed applications. It uses two high speed CB process op-amps: Amplifier A3, the output amplifier, is an AD847. The input amplifier (A1 and A2) is an AD827, which is a dual version of the AD847. This circuit has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.

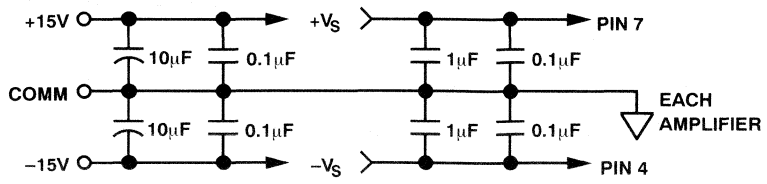


Input Frequency	CMRR
100 Hz	88.3 dB
1 kHz	87.4 dB
10 kHz	86.2 dB
100 kHz	67.4 dB
1 MHz	47.1 dB
10 MHz	26.4 dB

Bandwidth, Settling Time and Total Harmonic Distortion vs. Gain

Gain	R_G	C_{ADJ} (pF)	Small Signal Bandwidth	Settling Time to 0.1%	THD+Noise Below Input Level @ 10 kHz
1	Open	2–8	16.1 MHz	200 ns	82 dB
2	2 kΩ	2–8	14.7 MHz	200 ns	82 dB
10	226 Ω	2–8	4.5 MHz	370 ns	81 dB
100	20 Ω	2–8	660 kHz	2.5 μs	71 dB

Figure 23. A High Speed In-Amp Circuit for Data Acquisition



Input Frequency	CMRR
100 Hz	64.6 dB
1 MHz	44.7 dB
10 MHz	23.9 dB

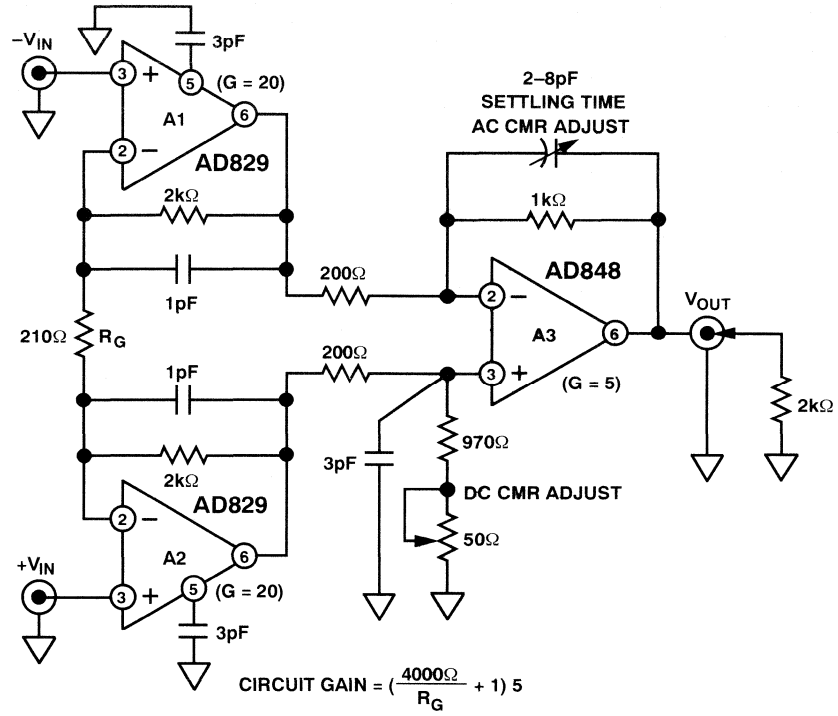


Figure 24. A High Gain, Video Bandwidth Three Op-Amp In-Amp Circuit

A High Gain, Video Bandwidth Three Op-Amp In-Amp

Figure 24 shows another three op-amp instrumentation amplifier circuit; this time two high speed externally compensated op-amps have been used for the input amplifiers.

This circuit provides a gain of 100 at video bandwidths. At a circuit gain of 100 the small signal bandwidth equals 18 MHz into an FET probe. Small signal bandwidth equals 6.6 MHz with a 50 Ω load. 0.1% settling time is 300 ns.

The input amplifiers operate at a gain of 20, while the output op-amp runs at a gain of 5. In this circuit the main bandwidth limitation is the gain/bandwidth product of the output amplifier. Extra care needs to be taken while breadboarding this circuit, since even a couple of extra picofarads of stray capacitance at the compensation pins of A1 and A2 will degrade circuit bandwidth.

Miscellaneous Applications

Stacking Instrumentation Amplifiers to Lower Noise

The signal-to-noise ratio of an amplification system can be improved by stacking two or more amplifiers together. Stacking refers to a connection where the inputs of two amplifiers are tied together, in parallel, while their outputs are connected in series. In this configuration, the combined signal-to-noise ratio will improve directly as the square root of the number of amplifiers being stacked. This improvement occurs because at the output the signals add arithmetically, while, at the input, their combined noise only increases as the square root of the number of amplifiers used. Note, however, that this improvement only occurs if the source voltage is not decreased by loading.

Using op-amps, a stacked connection is generally impractical since you need a third amplifier to sum the signals together. However, with instrumentation amplifiers, you simply connect one amplifier's output to the reference pin of the other. Figure 25 shows two AD524 instrumentation amplifiers connected in a stacked configuration, providing a 3 dB improvement in signal-to-noise ratio as compared to a single amplifier.

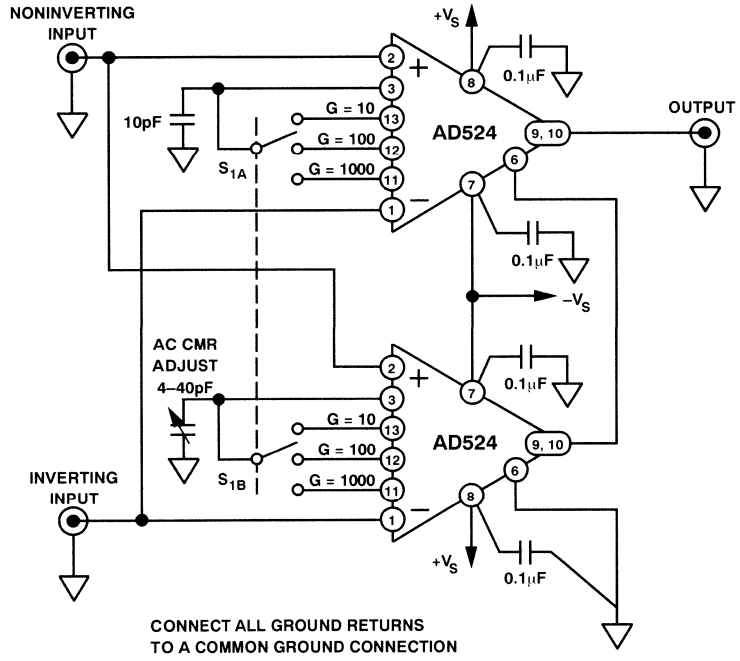


Figure 25. Two Instrumentation Amplifiers in a "Stacked" Configuration

The circuit of Figure 26 provides the same improvement in signal-to-noise ratio. It is not stacked, since its output is differential and effectively adds the two output signals together.

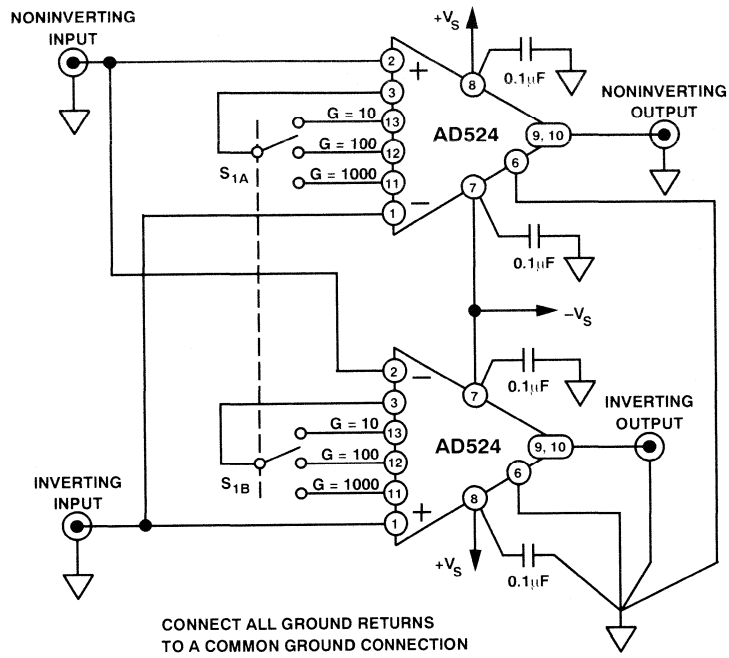


Figure 26. An Active Balanced Transformer Using "Stacked" Amplifiers

Table 3. Comparative Performance of Stacked Amplifier and Active Transformer Circuits

Parameter	Stacked Amplifier	Active Balanced Transformer
Slew Rate	5 V/μs	10 V/μs
Max Output Level	20 V p-p (7.1 V rms)	40 V p-p (14.2 V rms)
−3 dB Bandwidth ± 1 V p-p Output		
For Gain = 2 (6 dB)	dc–850 kHz	dc–1 MHz
For Gain = 20 (26 dB)	dc–380 kHz	dc–500 kHz
For Gain = 200 (46 dB)	dc–200 kHz	dc–200 kHz
For Gain = 2000 (66 dB)	dc–30 kHz	dc–30 kHz
Common-Mode Rejection Ratio (Gain = 2. 20 V p-p Sine Wave Common-Mode Input Level)	−80 dB at 60 Hz −80 dB at 10 kHz (with CMR Trim)	−93 dB at 60 Hz −83 dB at 10 kHz
Total Harmonic Distortion @ 1 kHz	<0.01%	<0.01%

Table 3 compares the performance of the two circuits. Note that the circuit of Figure 26 does not provide galvanic isolation between its input and output, unless both inputs are ac coupled. If ac input coupling is used, then two high value resistors, one connected between each AD524 input pin and ground, must be provided to permit a dc ground return. Without these resistors, the "unbled" input bias currents would quickly shut off (or saturate) the amplifiers.

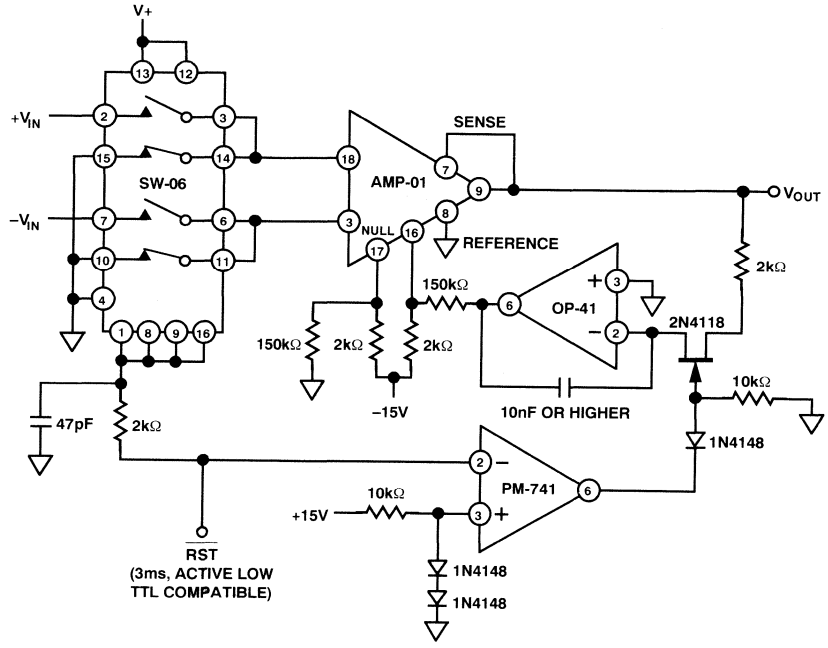


Figure 27. A Zero Drift Instrumentation Amplifier

A Zero Drift Instrumentation Amplifier

Amplifier offset voltages and drift can be reduced to negligible levels by using an "auto-zero" method. Such a circuit is shown in Figure 27. Unlike noisy chopper amplifiers, this method of offset correction puts the "zero" time under user control and with this scheme, the zeroing mechanism does not interfere with signal measurements. That is, this circuit goes into a zeroing mode when the user asserts a logic low for a least 3 ms to the RST input.

An AMP-01 in-amp is repeatedly servoed to provide an essentially zero output offset. When the RST input is "low," the 2N4118 J-FET transistor is turned on and the SW-06 analog switch connects both of the in-amp circuits' inputs to ground. The OP-41 then servos one of the AMP-01's null pins, forcing the AMP-01's output very close to zero (within the input offset range of the OP-41). When the RST input goes high, the SW-06 reconnects the signal inputs, the 2N4118 FET turns off and the OP-41 acts as a sample and hold amplifier, keeping the AMP-01 output "zeroed."

Using this integrator method of zeroing, the AMP-01's output offset voltage is held below 1 mV over the military temperature range (about 1/2 LSB change on a 12-bit system). If the circuit gain is set to 1000, the equivalent output drift at the amplifier's input is 0.06 μV/°C.

Remote Load Sensing Technique

Many monolithic instrumentation amplifiers provide separate pins for their sense and reference nodes. This allows greater flexibility of remote load and ground sense, thus minimizing any errors due to parasitic voltage drops within the circuit. The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the in-amp output. Similarly, the reference terminal sets the reference voltage about which the in-amp's output will swing.

If heavy output currents are expected and if the load is situated some distance from the amplifier, voltage drops due to trace or wire resistance will cause error. These voltage drops are particularly troublesome when driving 50 ohm loads.

One solution is to have the sense and reference terminals sense the load remotely as shown in Figure 28. This method of connection puts the IR drops inside the feedback loop of the in-amp and virtually eliminates this source of error.

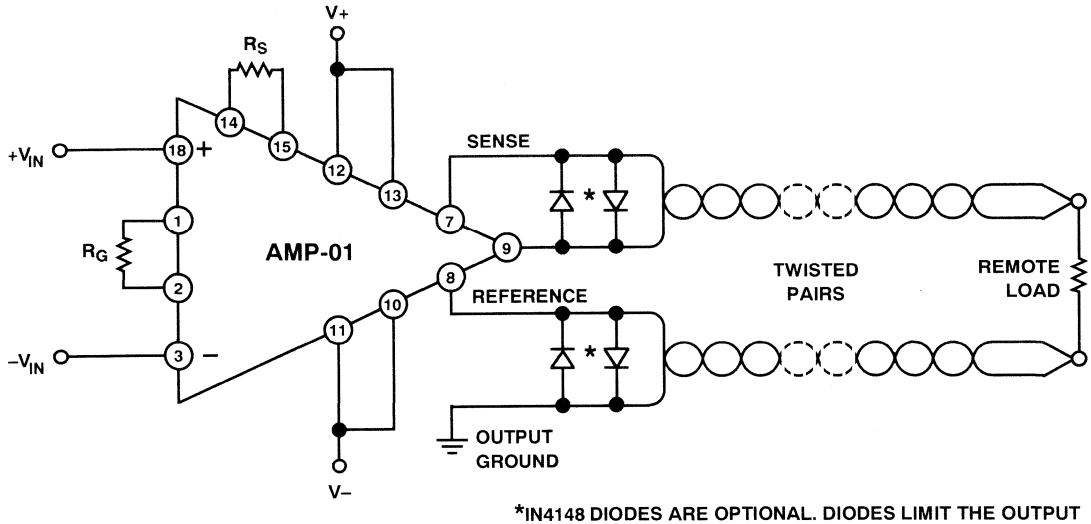


Figure 28. A Remote Load Sensing Connection

A 13-Bit Linear Bilateral Current Source

The circuit of Figure 29 shows how an instrumentation amplifier having separate sense and reference connections can be configured as a high precision bilateral current source, with a linearity of 0.01%. This current source will provide a full-scale output current of ±20 mA if the output voltage at the I_{OUT} pin is within the ±10 V compliance range.

A Precision Voltage-to-Current Converter

Figure 30 is a precision voltage-to-current converter whose scale factor is easily programmed for exact decade ratios using standard 1% metal film resistor values. The AD620 operates with full accuracy on standard ±5 volt power supply voltages. Furthermore, the quiescent current of the AD620 is only 900 μA.

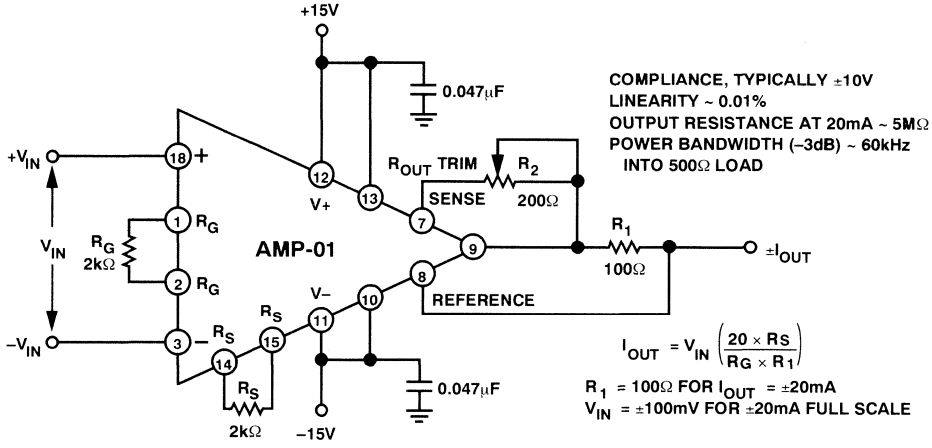


Figure 29. A 13-Bit Linear Bilateral Current Source

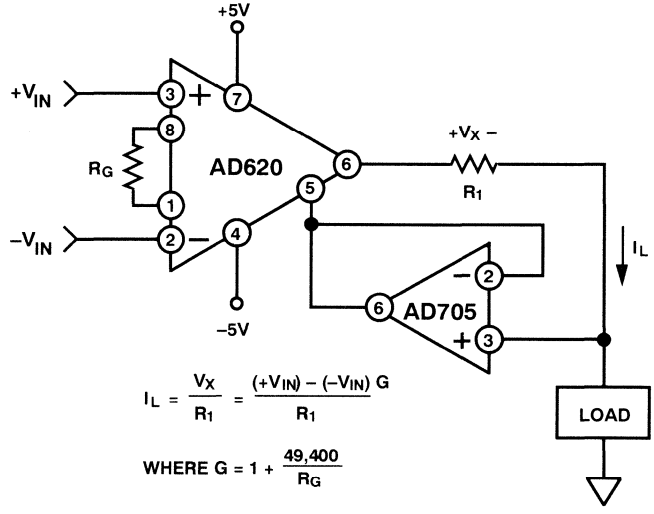


Figure 30. A Precision Voltage-to-Current Converter Which Operates on ±5 Volt Supplies

Current Sensor Interface

A typical current sensing application, making use of the large common-mode range of the AD626, is shown in Figure 31. The current being measured is sensed across resistor R_S. The value of R_S should be less than 1 kΩ and should be selected so that the average differential voltage cross this resistor is typically 100 mV.

To produce a full-scale output of +4 V, a gain of 40 is used, adjustable by ±20% to absorb the tolerance in the sense resistor. Note that there is sufficient headroom to allow at least a 10% overrange (to +4.4 V).

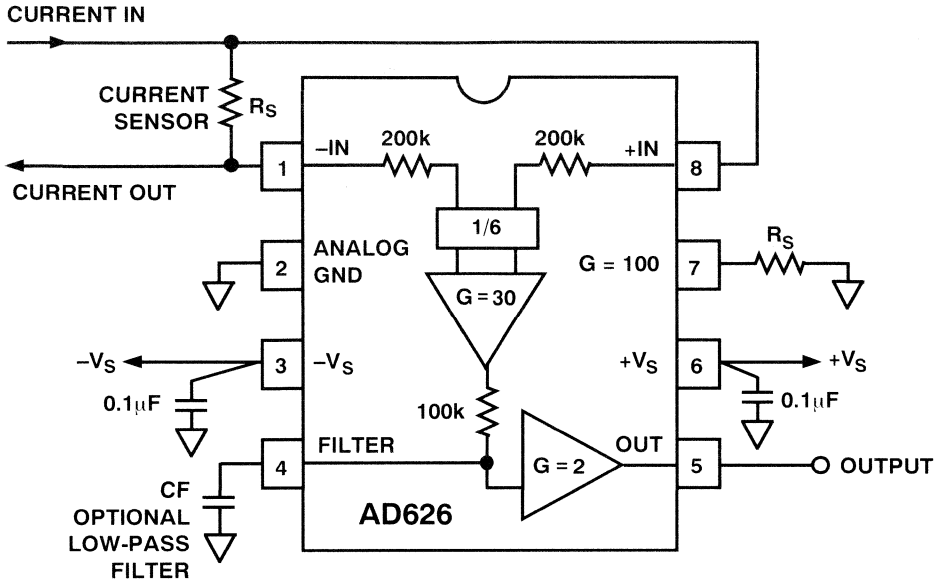


Figure 31. Current Sensor Interface

A High Performance Programmable Gain Amplifier

The excellent performance of the AD621 at a gain of 10 makes it a good choice to team up with the AD526 programmable gain amplifier (PGA) to yield a differential input PGA with gains of 10, 20, 40, 80, 160. As shown in Figure 32, the low offset of the AD621 allows total circuit offset to be trimmed using the offset null of the AD526, with only a negligible increase in total drift error. The total gain TC will be 9 ppm/°C max, with 2 μV/°C typical input offset drift. Bandwidth is 600 kHz for gains of 10 to 80, and 350 kHz at G = 160. Settling time is 13 μs to 0.01% for a 10V output step for all gains.

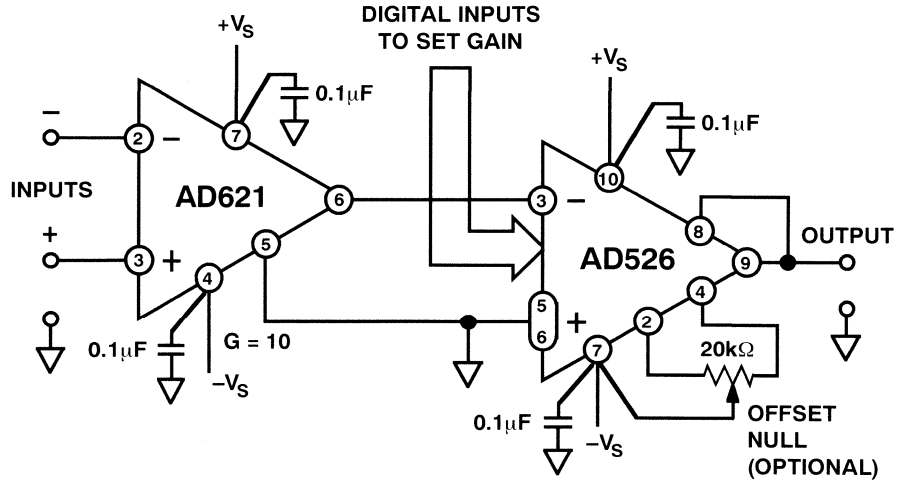


Figure 32. A High Performance Programmable Gain Amplifier

APPENDIX A

INSTRUMENTATION AMPLIFIER SPECIFICATIONS

To successfully apply any electronic component, a full understanding of its specifications is required. That is to say, the numbers contained in a spec sheet are of little value if the user doesn't have a clear picture of what each spec means. In this section, a typical monolithic instrumentation amplifier specification sheet will be reviewed. Some of the more important specifications will be discussed in terms of how they are measured and what errors they might contribute to the overall performance of the circuit.

Table 4 shows a portion of the specification sheet for the Analog Devices AD524 instrumentation amplifier.

Table 4. AD524 Specifications

A → **SPECIFICATIONS** (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

	Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524S Min	AD524S Typ	AD524S Max	Units
B →	GAIN										
	Gain Equation										
	(External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]$ ±20%			$\left[\frac{40{,}000}{R_G}+1\right]$ ±20%			$\left[\frac{40{,}000}{R_G}+1\right]$ ±20%		
C →	Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000		
D →	Gain Error										
	G = 1			**±0.05**			**±0.03**			**±0.05**	%
	G = 10			**±0.25**			**±0.15**			**±0.25**	%
	G = 100			**±0.5**			**±0.35**			**±0.5**	%
	G = 1000			**±2.0**			**±1.0**			**±2.0**	%
E →	Nonlinearity										
	G = 1			±0.01			±0.005			±0.01	%
	G = 10, 100			±0.01			±0.005			±0.01	%
	G = 1000			±0.01			±0.01			±0.01	%
F →	Gain vs. Temperature										
	G = 1			5			5			5	ppm/°C
	G = 10			15			10			10	ppm/°C
	G = 100			35			25			25	ppm/°C
	G = 1000			100			50			50	ppm/°C
G →	VOLTAGE OFFSET (May be Nulled)										
	Input Offset Voltage			**250**			**100**			**100**	µV
	vs. Temperature			**2**			**0.75**			**2.0**	µV/°C
	Output Offset Voltage			**5**			**3**			**3.0**	mV
	vs. Temperature			100			**50**			**50**	µV/°C
	Offset Referred to the Input vs. Supply										
	G = 1	**70**			75			75			dB
	G = 10	**85**			**95**			**95**			dB
	G = 100	**95**			**105**			**105**			dB
	G = 1000	**100**			**110**			**110**			dB
H →	INPUT CURRENT										
	Input Bias Current			**±50**			**±25**			**±50**	nA
	vs. Temperature		±100			±100			±100		pA/°C
	Input Offset Current			**±35**			**±15**			**±35**	nA
	vs. Temperature		±100			±100			±100		pA/°C

Table 4. AD524 Specifications (Continued)

INPUT				
Input Impedance				
Differential Resistance	10^9	10^9	10^9	Ω
Differential Capacitance	10	10	10	pF
Common Mode Resistance	10^9	10^9	10^9	Ω
Common Mode Capacitance	10	10	10	pF
Input Voltage Range				
Max Differ. Input Linear (V_{DL})[1]	**±10**	**±10**	**±10**	V
Max Common Mode Linear (V_{CM})	**$12V - \left(\frac{G}{2} \times V_D\right)$**	**$12V - \left(\frac{G}{2} \times V_D\right)$**	**$12V - \left(\frac{G}{2} \times V_D\right)$**	V
I → Common Mode Rejection dc				
to 60Hz with 1kΩ Source Imbalance				
G = 1	**70**	**75**	**70**	dB
G = 10	**90**	**95**	**90**	dB
G = 100	**100**	**105**	**100**	dB
G = 1000	**110**	**115**	**110**	dB
OUTPUT RATING				
V_{OUT}, R_L = 2kΩ	±10	±10	±10	V
DYNAMIC RESPONSE				
Small Signal −3dB				
G = 1	1	1	1	MHz
G = 10	400	400	400	kHz
G = 100	150	150	150	kHz
G = 1000	25	25	25	kHz
Slew Rate	5.0	5.0	5.0	V/μs
J → Settling Time to 0.01%, 20V Step				
G = 1 to 100	15	15	15	μs
G = 1000	75	75	75	μs

(A) Conditions

At the top of the spec sheet is the statement that the listed specs are typical @ $V_S = \pm 15$ V, $R_L = 2$ kΩ and $T_A = +25°C$ unless otherwise specified. This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature) the significant effects are usually indicated within the specs. This statement also tells us that all numbers are typical unless noted; "typical" means that the manufacturers characterization process has shown this number to be average, but individual devices may vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Those specs do not apply uniquely to instrumentation amplifiers.

(B) Gain

These specifications relate to the transfer function of the device. The gain equation of the AD524 is:

$$Gain = \frac{40{,}000\ \Omega}{R_G} + 1$$

To select an R_G for a given gain, solve the equation for R_G:

$$R_G = \frac{40{,}000\ \Omega}{G-1}$$

For example, the calculated resistance and the closest standard value for some common gains:

$G = 1$: $R_G = \infty$ *(Open Circuit)*
$G = 10$: $R_G = 4{,}444\ \Omega$ *(cal) or* $4.42\ k\Omega$
$G = 100$: $R_G = 404\ \Omega$ *(cal) or* $402\ \Omega$
$G = 1000$: $R_G = 40.04\ \Omega$ *(cal) or* $40.2\ \Omega$

Note that there will be a gain error due to the standard resistance values being different from those calculated. In addition, the tolerance of the resistors used (normally 1% metal film) will also affect accuracy. Of course the user must provide a very clean (low leakage) circuit board to realize an accurate gain of 1, since even a 200 MΩ leakage resistance will cause a gain error of 0.1%!

Note that resistor tolerance must be taken into consideration. Normal metal film resistors are within 1% of their stated value which means that any two resistors could be as much as 2% different in value from one another. Thin-film resistors in monolithic integrated circuits have an absolute tolerance of only ±20%, however the matching between resistors on the same chip can be excellent: typically better than 0.1%.

(C) Gain Range

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many instrumentation amplifiers may (and in fact will) work at higher gains, but the manufacturer will not promise a specific level of performance. In practice, as the gain resistor becomes increasingly smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher gains impractical.

(D) Gain Error

The number given by this specification describes maximum deviation from the gain equation. Monolithic in-amps such as the AD624 have very low factory trimmed gain errors with its maximum error of ±0.05% at unity gain and ±2% at a gain of 1000 being typical for a high quality in-amp. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network, all contribute to the overall gain error.

If the data is eventually digitized and fed to an "intelligent system" (such as a microprocessor), it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

(E) Nonlinearity

Nonlinearity is defined as the deviation from a straight line on the plot of output versus input. Figure 33a shows the transfer function of a device with exaggerated nonlinearity. The magnitude of this error can be calculated by:

$$Nonlinearity = \frac{Actual\ Output - Calculated\ Output}{Rated\ Full-Scale\ Output\ Range}$$

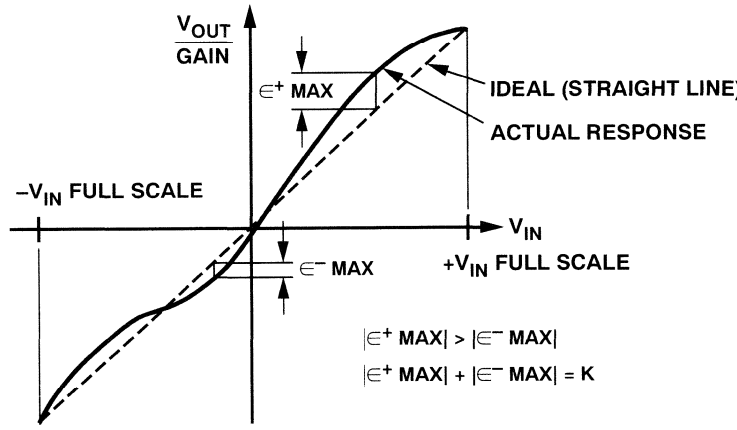


Figure 33a. Transfer Function Illustrating Exaggerated Nonlinearity

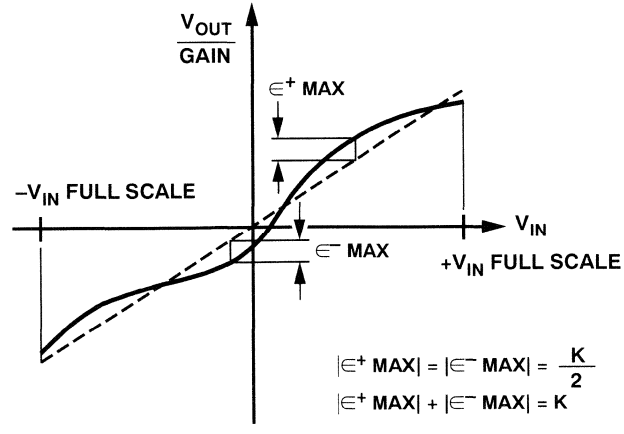


Figure 33b. The Transfer Function of Figure 33a After Calibration by Best-Straight-Line Method

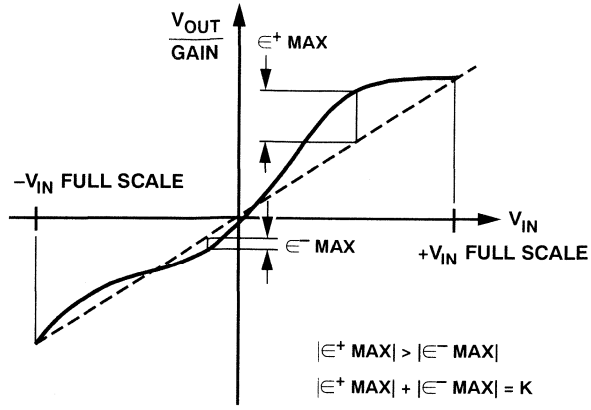


Figure 33c. The Transfer Function of Figure 33a After Calibration by End-Point Method

To confuse matters, this deviation can be specified relative to any straight line or to a specific straight line. There are two commonly used methods of specifying this ideal straight line relative to the performance of a precision measurement device.

The "Best Straight Line" method of nonlinearity specification consists of measuring the peak positive and peak negative deviations and then adjusting the slope of the device transfer function (by adjusting the gain and offset) so that these maximum positive and negative errors are equal. This method yields the best specifications but is difficult to implement because it requires that the user examine the entire output signal range to determine these maximum positive and negative deviations. The results of a best-straight-line calibration is shown by the transfer function of Figure 33b.

The "End-Point" method of specifying nonlinearity requires that the user perform his offset and/or gain calibrations at the extremes of the output range. This is much easier to implement but may result in nonlinearity errors of up to twice those attained with best-straight-line techniques. This worst case error will occur when the transfer function is "bowed" in one direction only. Figure 33c shows the results of end-point calibration.

Most linear devices, such as instrumentation amplifiers, are specified for best-straight-line linearity. This needs to be considered when evaluating the error budget for a particular application.

Regardless of the method used to specify nonlinearity, the errors thus created are irreducible. That is to say: these are neither fixed errors nor are they proportional to input or output voltage and,therefore, **cannot** be reduced by adjustment.

(F) Gain vs. Temperature

These numbers give both maximum and typical deviations from the gain equation as a function of temperature. An intelligent system can correct for this with an "auto-gain" cycle (measure a reference and renormalize).

(G) Voltage Offset

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift referred to both input and output. Input offset is that component of offset that is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater that at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

(H) Input Current

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. FET input-devices have lower bias currents, but those currents increase dramatically with temperature, doubling approximately every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, which will cause the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

(I) Common-Mode Rejection

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for both a full-range input voltage change and for a specified source imbalance. Common-mode rejection ratio (CMRR) is a ratio expression while common-mode rejection (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In most IAs, the CMRR increases with gain. This is because most designs have a front-end configuration that does not amplify common-mode signals. Since the standard for CMRR specifications is referred to the output (RTO), a gain for differential signals in the total absence of gain for common-mode input signals will yield a 1-to-1 improvement of CMRR with gain. For example, if an instrumentation amplifier provides a CMR of 60 dB at unity gain, then increasing the amplifier's gain to 10 will increase the differential gain 10 times. But, (ideally) the common-mode gain will remain at unity. Therefore, the CMR is now 80 dB—a direct improvement with gain.

This means that the common-mode output error signal will not increase with gain, it does not mean that it decreases with gain! At higher gains, however, amplifier bandwidth does decrease. Since differences in phase shift through the differential input stage will show up as a common-mode error, CMRR becomes more frequency dependent at high gains.

(J) Settling Time

Settling time is defined as that length of time required for the output voltage to approach and remain within a certain tolerance of its final value. It is usually specified for a fast full-scale input step and includes output slewing time. Since several factors contribute to the overall setting time, fast settling to 0.1% doesn't necessarily mean proportionally fast-settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors include slew rate limiting, under-damping (ringing) and thermal gradients (long tails).

Error Budget Analysis

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 34 shows a differential transducer, unbalanced by 100 Ω, supplying a 0 to 20 millivolt signal to an AD524C. The output of the IA feeds a 14-bit A-to-D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature (ΔT) within the operating range is from ambient to +85°C (85°C–25°C = 60°C).

The input signal must be amplified by a factor of 10 in order to utilize the full resolution of the A-to-D converter. Solving the gain equation for G = 10 gives a value of 22.22 kΩ for R_G.

Table 5 lists all applicable error sources and their corresponding effects on accuracy. Initial errors are defined as those errors that can be reduced to a negligible amount by performing an initial calibration.

Reducible errors include these initial errors along with other errors that occur during normal operation that may be corrected by an adaptive or "intelligent" system. For example, changes in gain or offset may be measured during an auto-zero/auto-gain cycle by measuring two known voltages (a precision reference and ground, for example). This is a common practice in computer or processor-controlled equipment.

Irreducible errors are errors are those which cannot be readily corrected either at initial calibration or during use. It can be argued that an array of preci-

Table 5. An Error Budget Analysis of an AD524 In-Amp in a Bridge Application

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy @ T_A = 25°C	Effect on Absolute Accuracy @ T_A = 85 °C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500 ppm	2500 ppm	2500 ppm	–
Gain Instability	25 ppm	(25 ppm/°C)(60°C) = 1500 ppm	–	1500 ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30 ppm	–	–	30 ppm
Input Offset Voltage	±50 μV, RTI	±50 μV/20 mV = ±2500 ppm	2500 ppm	2500 ppm	–
Input Offset Voltage Drift	±0.5 μV/°C	(±0.5 μV/°C) (60°C) = 30 μV			
		30 μV/20 mV = 1500 ppm	–	1500 ppm	–
Output Offset Voltage[1]	±2.0 mV	±2.0 mV/20 mV = 1000 ppm	1000 ppm	1000 ppm	–
Output Offset Voltage Drift[1]	±25 μV/°C	(±25 μV/°C)(60°C) = 1500 μV			
		1500 μV/20 mV = 750 ppm	–	750 ppm	–
Bias Current—Source	±15 nA	(±15 nA)(100 Ω) = 1.5 μV			
Imbalance Error		1.5 μV/20 mV = 75 ppm	75 ppm	75 ppm	–
Bias Current—Source	±100 pA/°C	(±100 pA/°C)(100 Ω)(60°C) = 0.6 μV			
Imbalance Drift		0.6 μV/20 mV = 30 ppm	–	30 ppm	–
Offset Current—Source	±10 nA	(±10 nA)(100 Ω) = 1 μV			
Imbalance Error		1 μV/20 mV = 50 ppm	50 ppm	50 ppm	–
Offset Current—Source	±100 pA/°C	(±100 pA/°C)(100 Ω)(60°C) = 0.6 μV			
Imbalance Drift		0.6 μV/20 mV = 30 ppm	–	30 ppm	–
Offset Current—Source	±10 nA	(±10 nA)(175 Ω) = 3.5 μV			
Resistance—Error		3.5 μV/20 mV = 87.5 ppm	87.5 ppm	87.5 ppm	–
Offset Current—Source	±100 pA/°C	(±100 pA/°C)(175 Ω)(60°C) = 1 μV			
Resistance—Drift		1 μV/20 mV = 50 ppm	–	50 ppm	–
Common-Mode Rejection	115 dB	115 dB = 1.8 ppm × 5 V = 8.8 μV			
5 V dc		8.8 μV/20 mV = 444 ppm	444 ppm	444 ppm	–
Noise, RTI					
(0.1 Hz–10 Hz)	0.3 μV p-p	0.3 μV p-p/20 mV = 15 ppm	–	–	15 ppm
		Total Error	6656.5 ppm	10516.5 ppm	45 ppm

NOTE

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

sion references would permit a software linearity correction, but in most applications that would be unrealistically cumbersome.

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in its value. In these applications, only the irreducible errors (45 ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A-to-D output, the additional auto-gain/auto-zero cycle will remove all reducible errors and may also eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

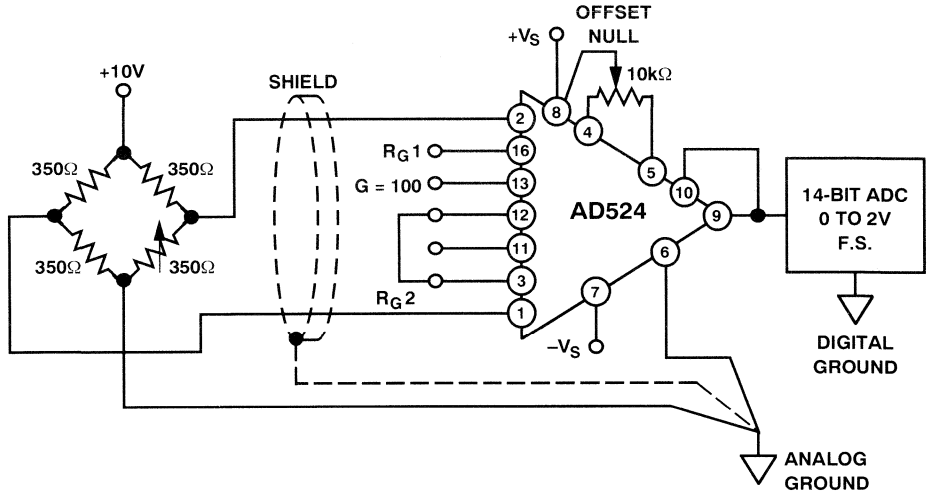


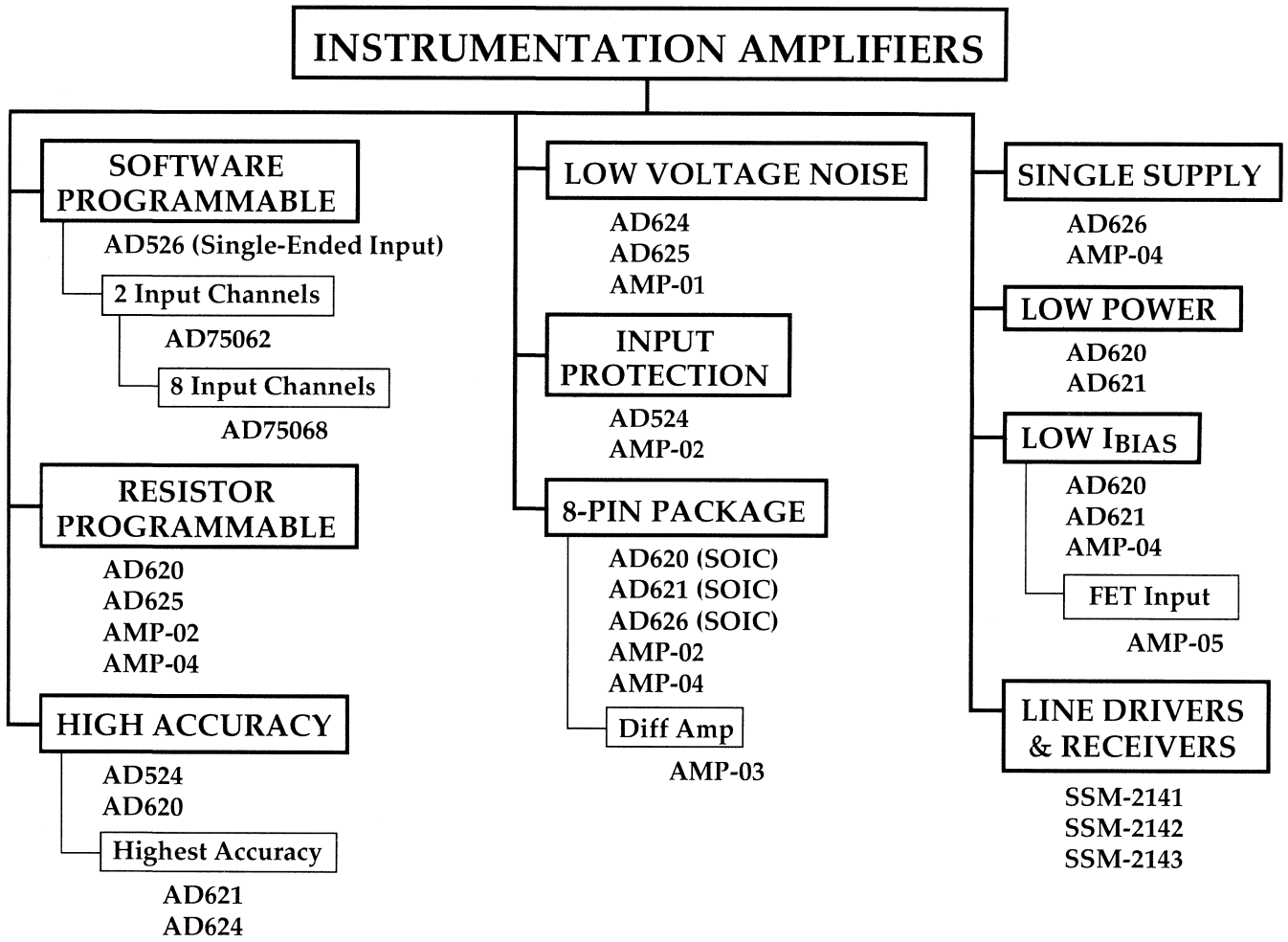
Figure 34. Typical Bridge Application

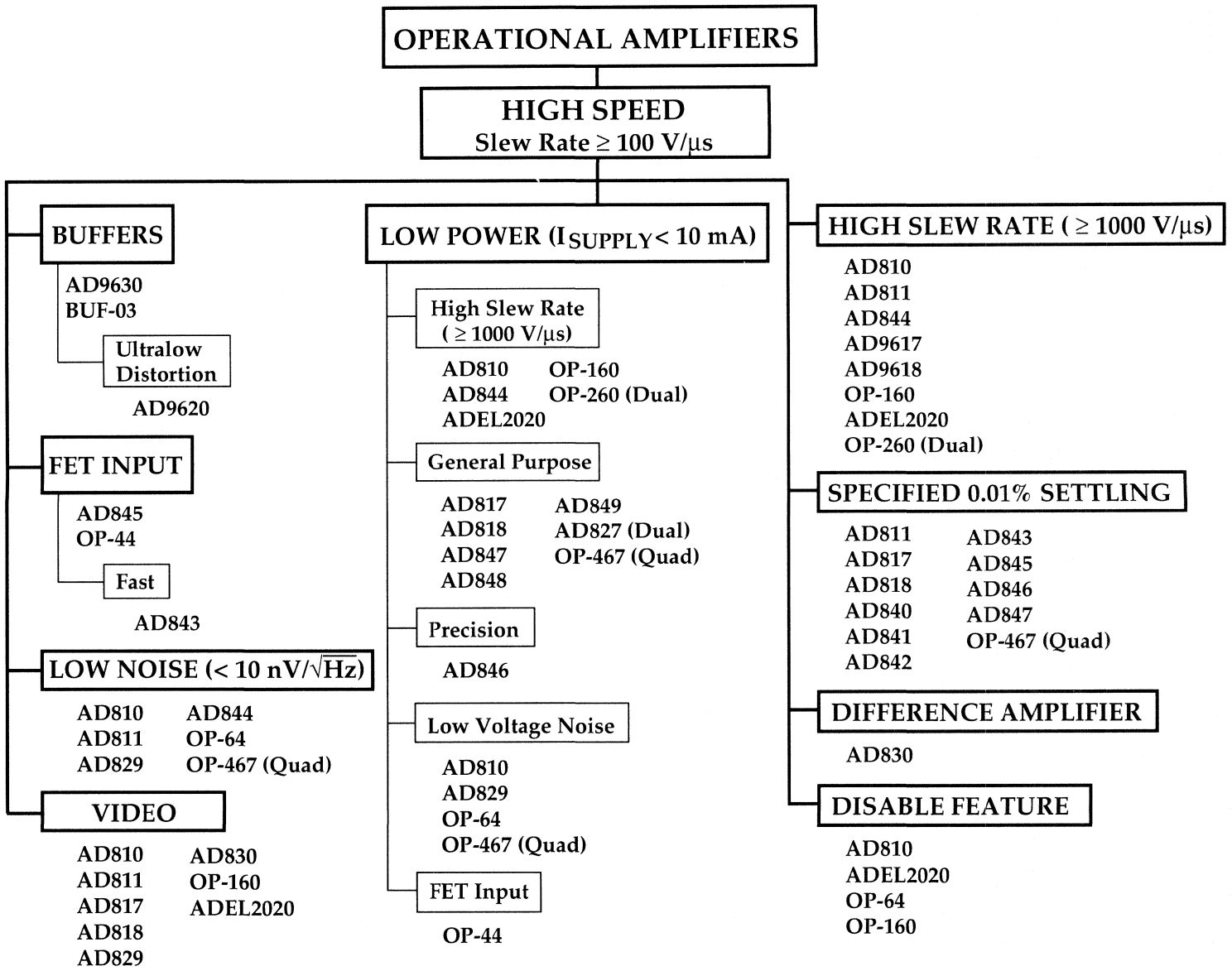
APPENDIX B

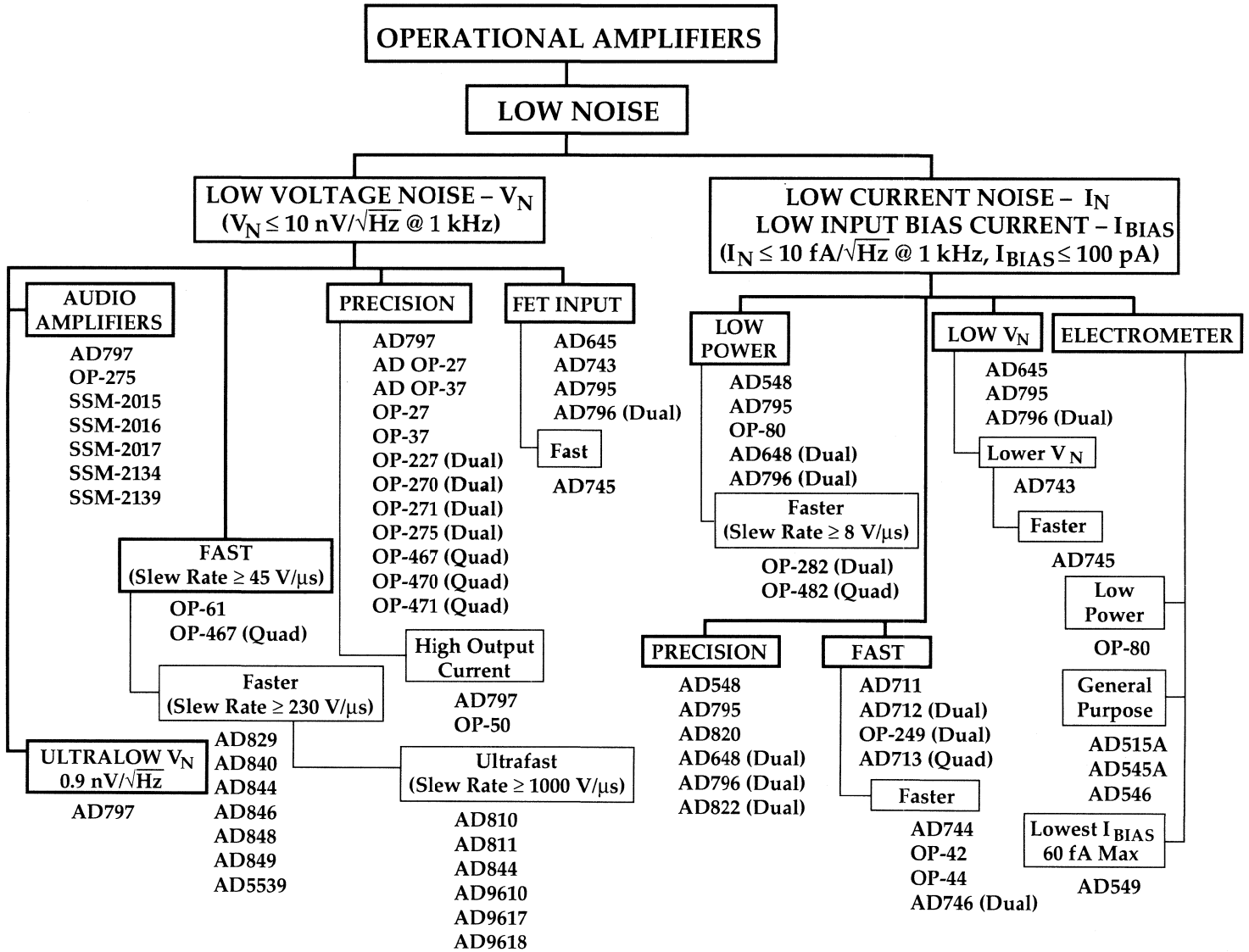
MONOLITHIC INSTRUMENTATION AMPLIFIERS AVAILABLE FROM ANALOG DEVICES

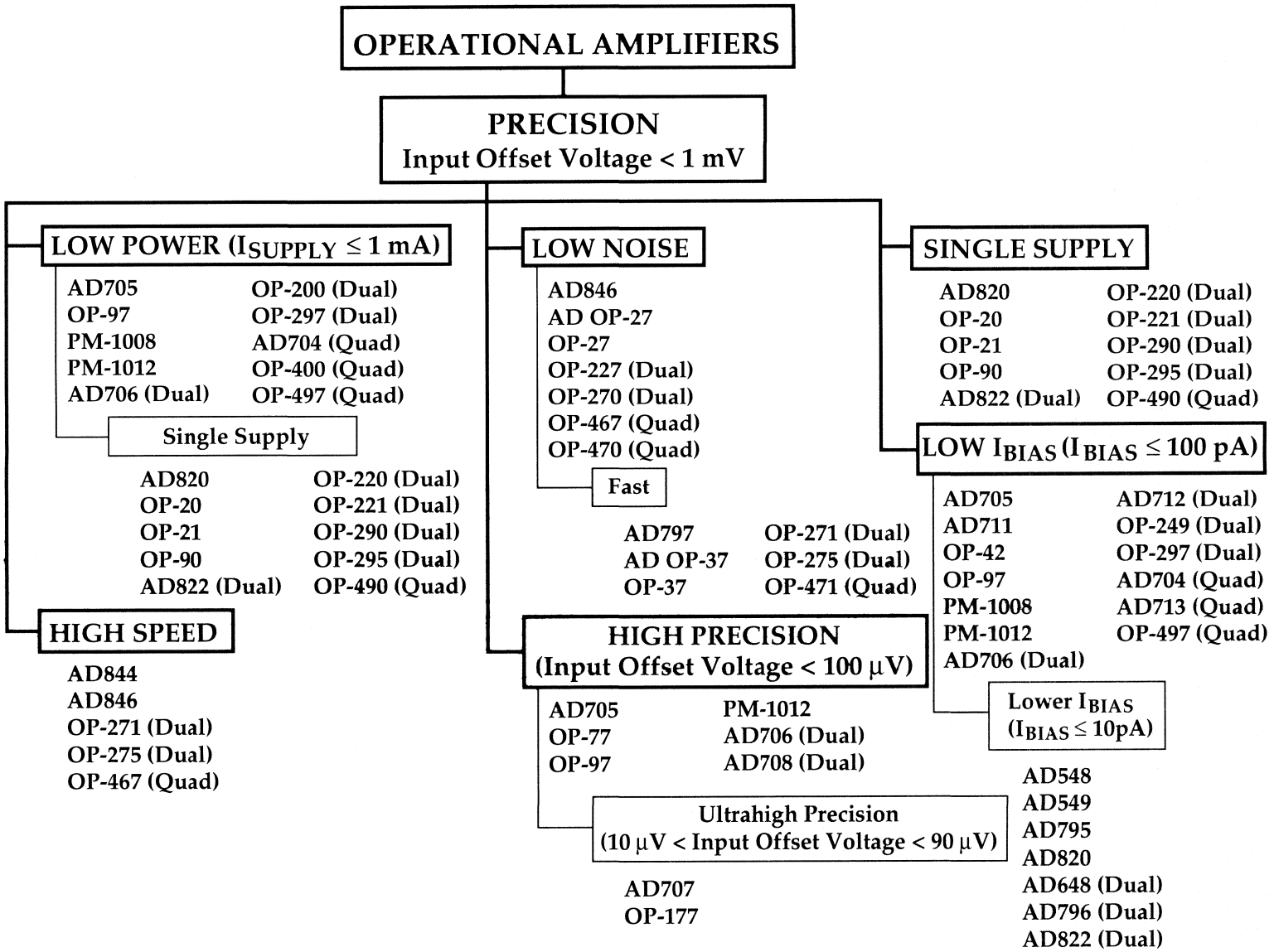
Model	Gain Sel[1]	Gain Range	Gain Error % Max	Gain T.C. ppm/°C Max	Bandwidth (Gain = 1)	Package Options[2]	Temp Range[3]
AD524	P	1, 10, 100, 1k	0.02–2.0	5–100	1 MHz	D, E, R	I, M
AD526	SP	1, 2, 4, 8, 16	0.01–0.15	2–5	4 MHz	D, N	C, I, M
AD620	RP	1–10k	0.02–0.7	50	1 MHz	N, Q, R	I, M
AD621	P	10, 100	0.05–0.15	5	800 kHz (G = 10)	N, Q, R	I, M
AD624	P	1, 100 200, 500, 1k	0.02–1.0	5–25	1 MHz	D	I, M
AD625	RP	1–10k	0.02–0.05	5	650 kHz	D, N	C, I, M
AD626	P	1–160	0.2	55	150 kHz	N, Q, R	I, M
AD365	SP	1, 10, 100, 500	0.05–0.1	5–10	800 kHz	M	I
AD522*	RP	1–10k	0.05–1.0	2–50	300 kHz	D	I, M
AD521*	RP	0.1–1k	0.25–3.0	3–50	2	D	C, M
AMP-01	RP	0.1–10k	0.6–0.8	10–15	570 kHz	E, Q, N	C, I, M
AMP-02	RP	1–10k	0.5–0.7	50	1.2 MHz	N, R	I
AMP-03	N/A	G = 1	0.008–0.015	15 typ	3 MHz	N	I
AMP-04	RP	1–1k	0.5	5 typ	300 kHz	N, Q, R	I, M
AMP-05	RP	0.1–2k	0.5–1.0	10–20	3 MHz	Q	I, M
SSM-2017**	RP	1–1k	0.13–2.7 typ	N/A	3.5 MHz	N	I

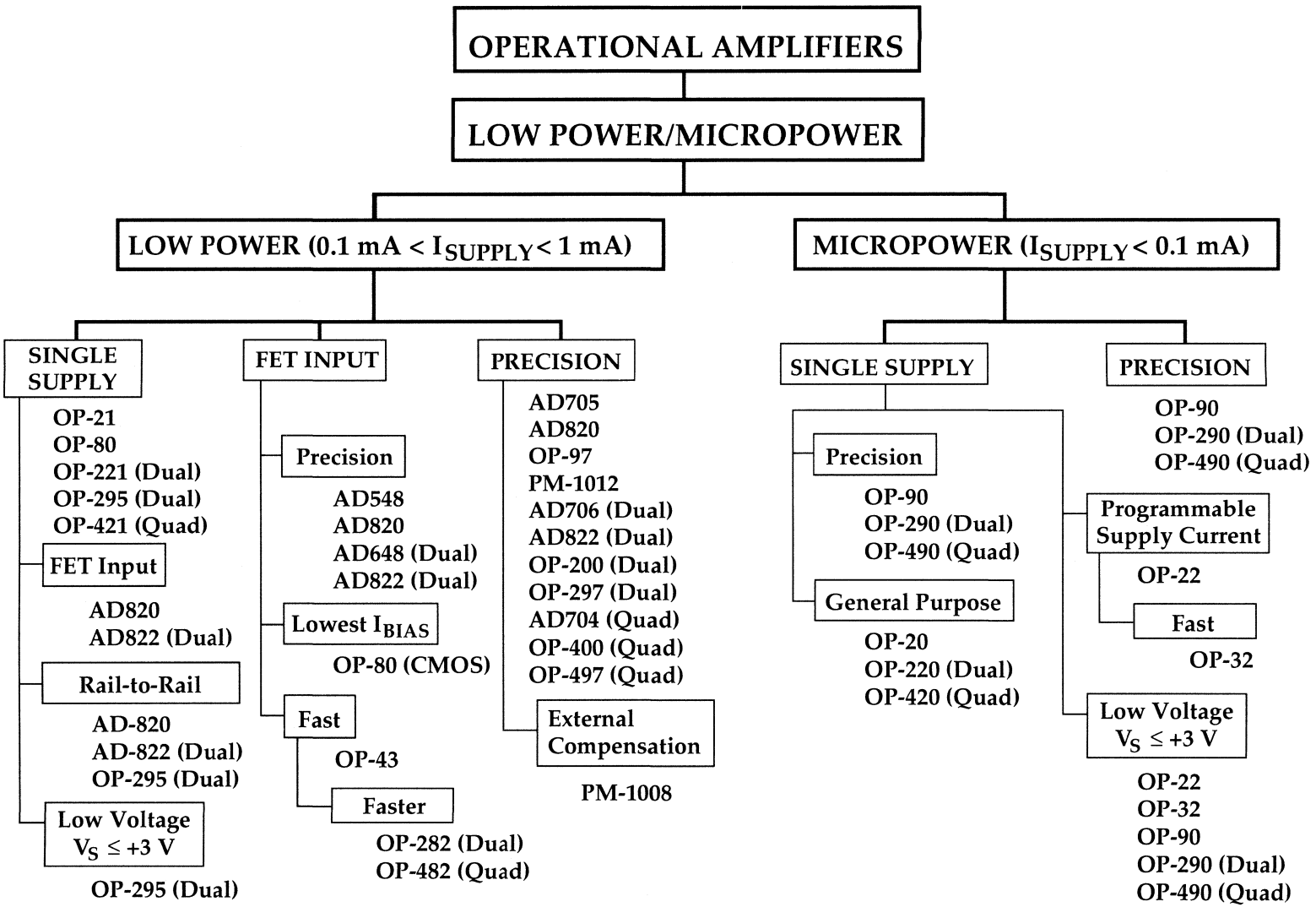
NOTES
*Not recommended for new designs.
**This device is optimized for use as a low noise audio preamplifier.
[1]Gain Selection: P–pin programmable; SP–software programmable; RP–resistor programmable.
[2]Package options: D–side-brazed dual-in-line ceramic; E–leadless ceramic chip carrier; M–metal hermetic dual-in-line; N–plastic molded dual-in-line; Q–cerdip package; R–surface mount package.
[3]Temperature ranges: C–commercial (0°C to +70°C); I–industrial (−40°C to +85°C); M–military (−55°C to +125°C).


INSTRUMENTATION AMPLIFIERS
SOFTWARE PROGRAMMABLE
AD526 (Single-Ended Input)
2 Input Channels
AD75062
8 Input Channels
AD75068
RESISTOR PROGRAMMABLE
AD620
AD625
AMP-02
AMP-04
HIGH ACCURACY
AD524
AD620
Highest Accuracy
AD621
AD624
LOW VOLTAGE NOISE
AD624
AD625
AMP-01
INPUT PROTECTION
AD524
AMP-02
8-PIN PACKAGE
AD620 (SOIC)
AD621 (SOIC)
AD626 (SOIC)
AMP-02
AMP-04
Diff Amp
AMP-03
SINGLE SUPPLY
AD626
AMP-04
LOW POWER
AD620
AD621
LOW IBIAS
AD620
AD621
AMP-04
FET Input
AMP-05
LINE DRIVERS & RECEIVERS
SSM-2141
SSM-2142
SSM-2143


OPERATIONAL AMPLIFIERS
HIGH SPEED
Slew Rate ≥ 100 V/µs
BUFFERS
AD9630
BUF-03
Ultralow Distortion
AD9620
FET INPUT
AD845
OP-44
Fast
AD843
LOW NOISE (< 10 nV/√Hz)
AD810 AD844
AD811 OP-64
AD829 OP-467 (Quad)
VIDEO
AD810 AD830
AD811 OP-160
AD817 ADEL2020
AD818
AD829
LOW POWER (ISUPPLY < 10 mA)
High Slew Rate (≥ 1000 V/µs)
AD810 OP-160
AD844 OP-260 (Dual)
ADEL2020
General Purpose
AD817 AD849
AD818 AD827 (Dual)
AD847 OP-467 (Quad)
AD848
Precision
AD846
Low Voltage Noise
AD810
AD829
OP-64
OP-467 (Quad)
FET Input
OP-44
HIGH SLEW RATE (≥ 1000 V/µs)
AD810
AD811
AD844
AD9617
AD9618
OP-160
ADEL2020
OP-260 (Dual)
SPECIFIED 0.01% SETTLING
AD811 AD843
AD817 AD845
AD818 AD846
AD840 AD847
AD841 OP-467 (Quad)
AD842
DIFFERENCE AMPLIFIER
AD830
DISABLE FEATURE
AD810
ADEL2020
OP-64
OP-160


OPERATIONAL AMPLIFIERS
LOW NOISE
LOW VOLTAGE NOISE – V_N
($V_N \leq 10$ nV/$\sqrt{Hz}$ @ 1 kHz)
LOW CURRENT NOISE – I_N
LOW INPUT BIAS CURRENT – I_{BIAS}
($I_N \leq 10$ fA/$\sqrt{Hz}$ @ 1 kHz, $I_{BIAS} \leq 100$ pA)
AUDIO AMPLIFIERS
AD797
OP-275
SSM-2015
SSM-2016
SSM-2017
SSM-2134
SSM-2139
PRECISION
AD797
AD OP-27
AD OP-37
OP-27
OP-37
OP-227 (Dual)
OP-270 (Dual)
OP-271 (Dual)
OP-275 (Dual)
OP-467 (Quad)
OP-470 (Quad)
OP-471 (Quad)
FET INPUT
AD645
AD743
AD795
AD796 (Dual)
Fast
AD745
LOW POWER
AD548
AD795
OP-80
AD648 (Dual)
AD796 (Dual)
Faster (Slew Rate ≥ 8 V/μs)
OP-282 (Dual)
OP-482 (Quad)
LOW V_N
AD645
AD795
AD796 (Dual)
Lower V_N
AD743
Faster
AD745
ELECTROMETER
Low Power
OP-80
General Purpose
AD515A
AD545A
AD546
Lowest I_{BIAS} 60 fA Max
AD549
FAST (Slew Rate ≥ 45 V/μs)
OP-61
OP-467 (Quad)
Faster (Slew Rate ≥ 230 V/μs)
AD829
AD840
AD844
AD846
AD848
AD849
AD5539
Ultrafast (Slew Rate ≥ 1000 V/μs)
AD810
AD811
AD844
AD9610
AD9617
AD9618
High Output Current
AD797
OP-50
ULTRALOW V_N 0.9 nV/$\sqrt{Hz}$
AD797
PRECISION
AD548
AD795
AD820
AD648 (Dual)
AD796 (Dual)
AD822 (Dual)
FAST
AD711
AD712 (Dual)
OP-249 (Dual)
AD713 (Quad)
Faster
AD744
OP-42
OP-44
AD746 (Dual)


OPERATIONAL AMPLIFIERS
PRECISION
Input Offset Voltage < 1 mV
LOW POWER (ISUPPLY ≤ 1 mA)
AD705
OP-97
PM-1008
PM-1012
AD706 (Dual)
OP-200 (Dual)
OP-297 (Dual)
AD704 (Quad)
OP-400 (Quad)
OP-497 (Quad)
Single Supply
AD820
OP-20
OP-21
OP-90
AD822 (Dual)
OP-220 (Dual)
OP-221 (Dual)
OP-290 (Dual)
OP-295 (Dual)
OP-490 (Quad)
HIGH SPEED
AD844
AD846
OP-271 (Dual)
OP-275 (Dual)
OP-467 (Quad)
LOW NOISE
AD846
AD OP-27
OP-27
OP-227 (Dual)
OP-270 (Dual)
OP-467 (Quad)
OP-470 (Quad)
Fast
AD797
AD OP-37
OP-37
OP-271 (Dual)
OP-275 (Dual)
OP-471 (Quad)
HIGH PRECISION
(Input Offset Voltage < 100 μV)
AD705
OP-77
OP-97
PM-1012
AD706 (Dual)
AD708 (Dual)
Ultrahigh Precision
(10 μV < Input Offset Voltage < 90 μV)
AD707
OP-177
SINGLE SUPPLY
AD820
OP-20
OP-21
OP-90
AD822 (Dual)
OP-220 (Dual)
OP-221 (Dual)
OP-290 (Dual)
OP-295 (Dual)
OP-490 (Quad)
LOW IBIAS (IBIAS ≤ 100 pA)
AD705
AD711
OP-42
OP-97
PM-1008
PM-1012
AD706 (Dual)
AD712 (Dual)
OP-249 (Dual)
OP-297 (Dual)
AD704 (Quad)
AD713 (Quad)
OP-497 (Quad)
Lower IBIAS
(IBIAS ≤ 10pA)
AD548
AD549
AD795
AD820
AD648 (Dual)
AD796 (Dual)
AD822 (Dual)


OPERATIONAL AMPLIFIERS
LOW POWER/MICROPOWER
LOW POWER (0.1 mA < I_{SUPPLY} < 1 mA)
MICROPOWER (I_{SUPPLY} < 0.1 mA)
SINGLE SUPPLY
OP-21
OP-80
OP-221 (Dual)
OP-295 (Dual)
OP-421 (Quad)
FET Input
AD820
AD822 (Dual)
Rail-to-Rail
AD-820
AD-822 (Dual)
OP-295 (Dual)
Low Voltage $V_S \leq +3$ V
OP-295 (Dual)
FET INPUT
Precision
AD548
AD820
AD648 (Dual)
AD822 (Dual)
Lowest I_{BIAS}
OP-80 (CMOS)
Fast
OP-43
Faster
OP-282 (Dual)
OP-482 (Quad)
PRECISION
AD705
AD820
OP-97
PM-1012
AD706 (Dual)
AD822 (Dual)
OP-200 (Dual)
OP-297 (Dual)
AD704 (Quad)
OP-400 (Quad)
OP-497 (Quad)
External Compensation
PM-1008
SINGLE SUPPLY
Precision
OP-90
OP-290 (Dual)
OP-490 (Quad)
General Purpose
OP-20
OP-220 (Dual)
OP-420 (Quad)
PRECISION
OP-90
OP-290 (Dual)
OP-490 (Quad)
Programmable Supply Current
OP-22
Fast
OP-32
Low Voltage $V_S \leq +3$ V
OP-22
OP-32
OP-90
OP-290 (Dual)
OP-490 (Quad)

SUBJECT INDEX

DEVICE INDEX